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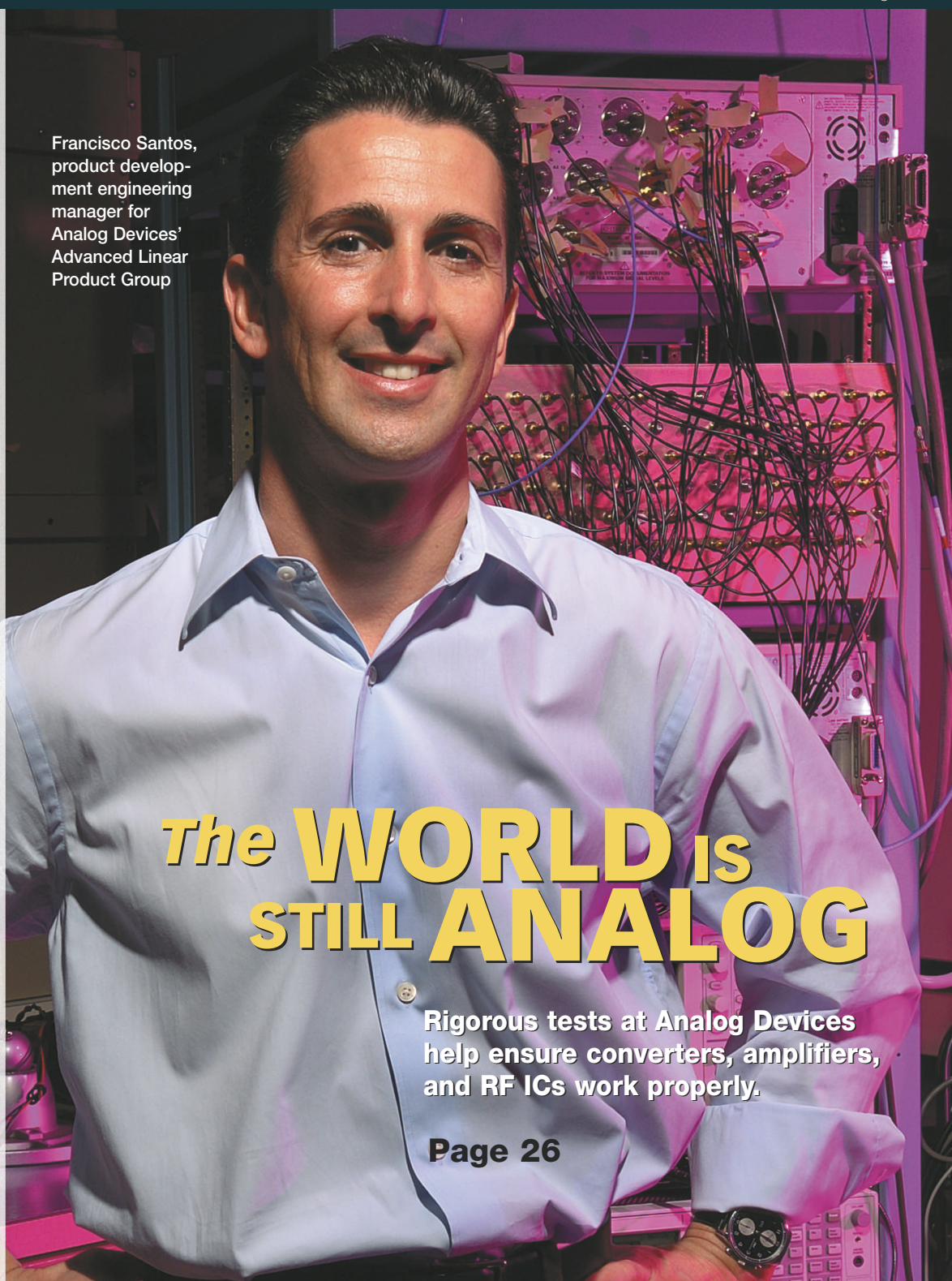

Francisco Santos, product development engineering manager for Analog Devices' Advanced Linear Product Group

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Rigorous tests at Analog Devices help ensure converters, amplifiers, and RF ICs work properly.

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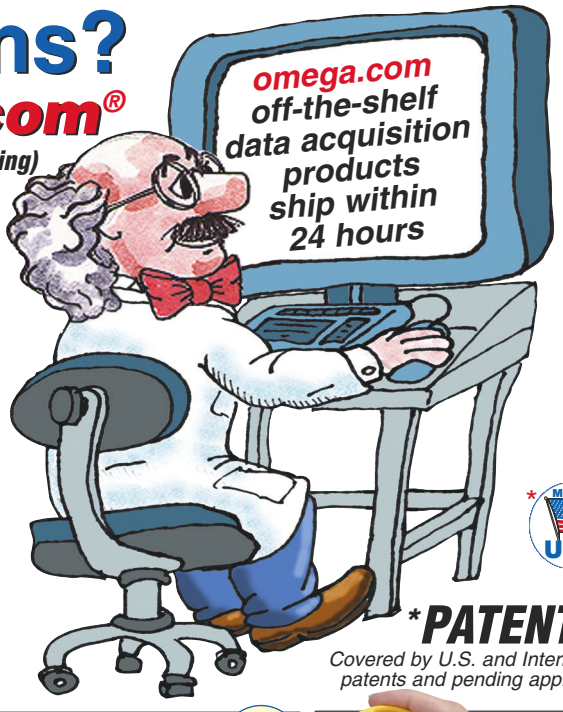

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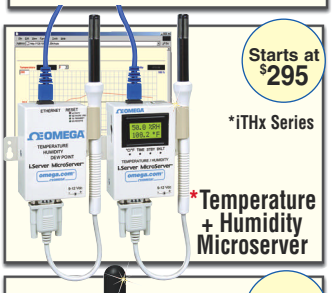

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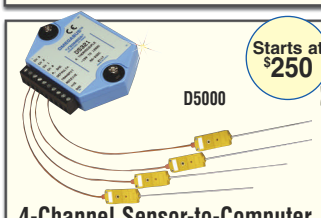

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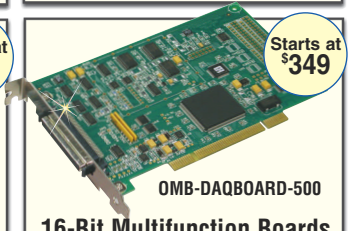

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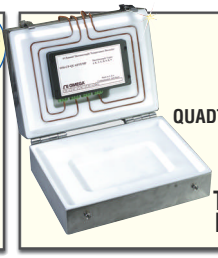

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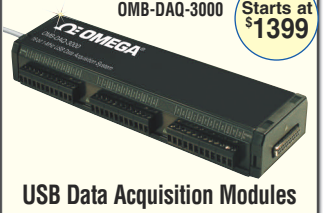

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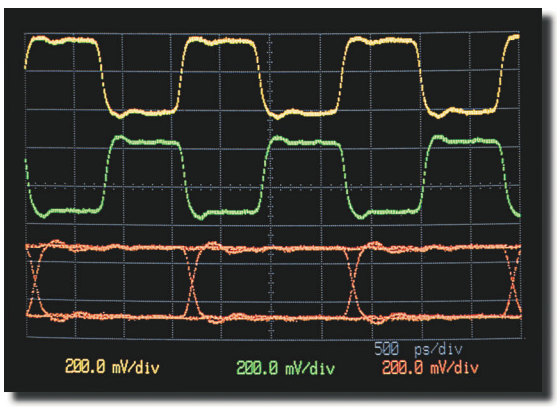

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COVER BY: MARK WILSON

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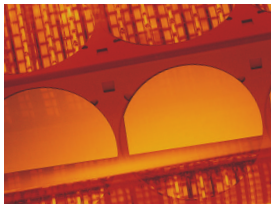

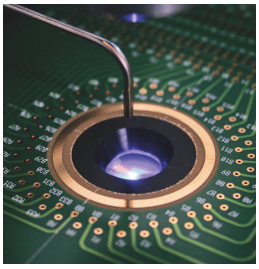

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Automotive & Aerospace Test Report

- **Weighing cost vs tolerances**
  In an exclusive interview, Larry Stockline, president of Promess, explained how his company improves manufacturing quality in automotive products by using looser tolerances. While it sounds counterintuitive, the concept is validated by the fact that Promess's systems produce high-quality parts for demanding Big 3 and transplant automakers.

- **Cold Regions Test Center supports US troops**
  We spoke with Jeffrey Lipscomb, technical director of the Cold Regions Test Center in Delta Junction, AK, to learn about the CRTC's role in testing vehicles and aircraft in preparation for theaters of engagements.

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A song for engineers struggling to make measurements

Senior technical editor Martin Rowe has written the new theme song for all overworked and underbudgeted test engineers. You can listen to his creation, "The Measurement Blues," on the *Test & Measurement World* Web site. Once you've listened to the recording, send us your comments as well as links to music you want to share with the T&M audience.

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"Taking the Measure" (blog commentary and links)

- Outsourcing's out as world goes online
- Speaking up for CO_2
- Amazon patent to face review
- Fraud taints Chinese DSP effort
- A CEO's misguided writing
- The future of design for test

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From the Archives

- **Test-system development: Do everything first**
  For this month's Test Voices column (p. 9), Martin Rowe interviewed Norman Kirchner of Texas Instruments to learn how the software infrastructure engineer manages his company's test code. When Kirchner previously worked at Engineering Specialists, he participated in a *T&MW*-sponsored panel discussion about the design of test systems. We covered the discussion in "Test-system development: Do everything first," in our February 2005 issue.

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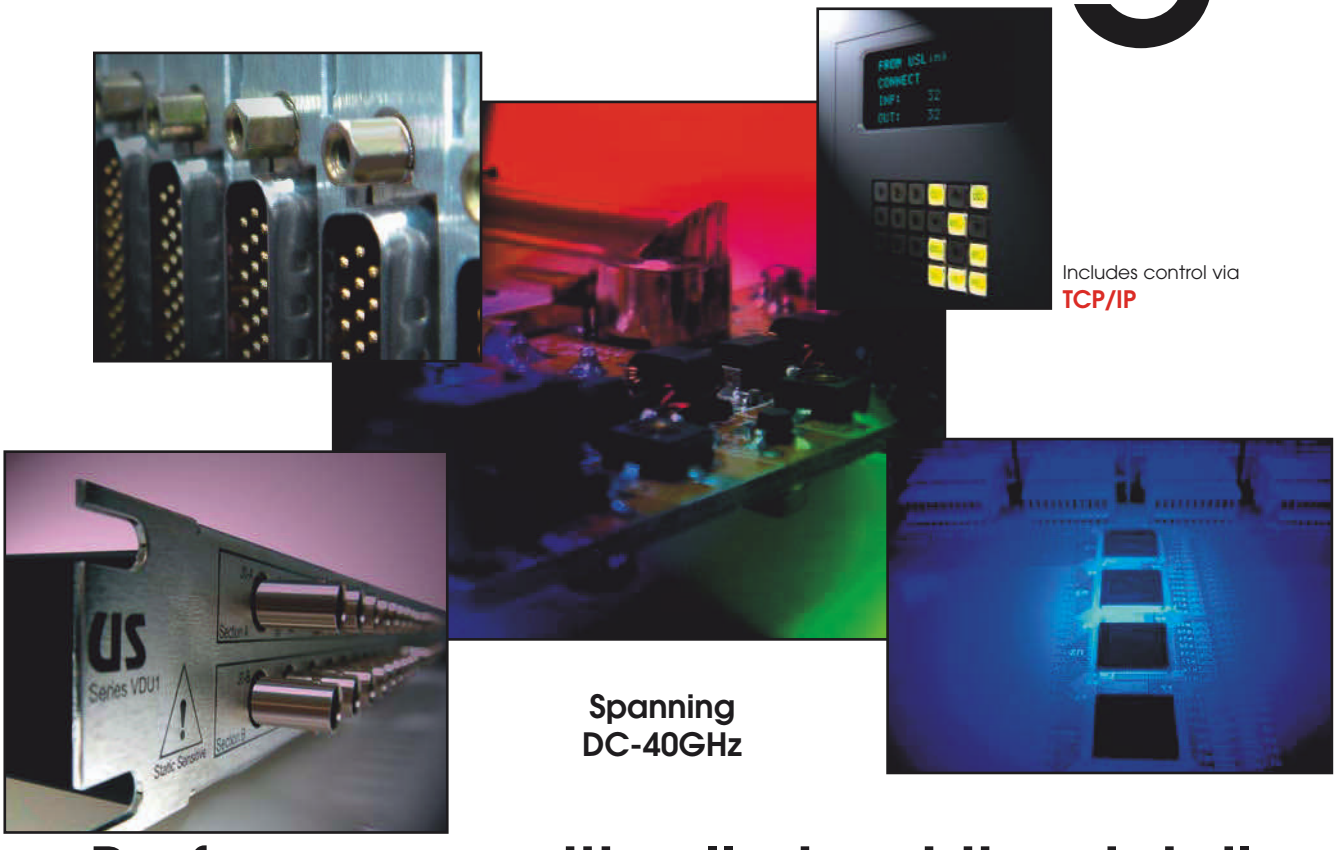
Switching?



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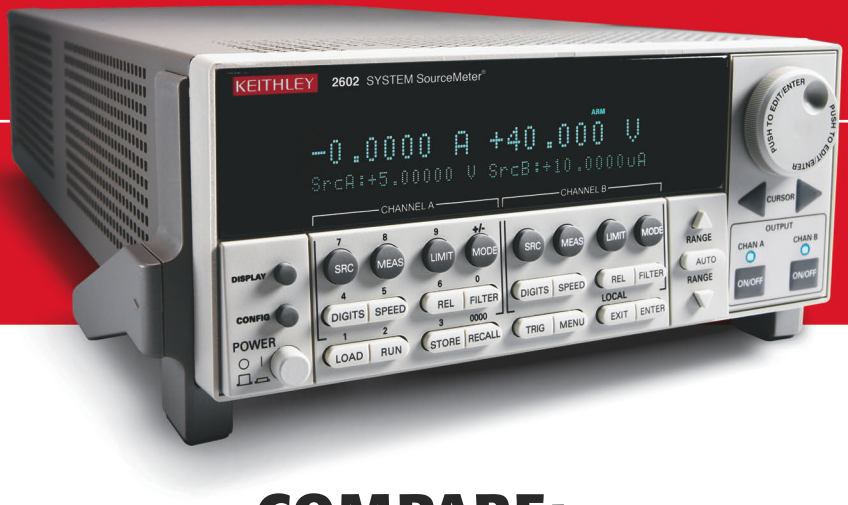

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Patent common sense

Patent trolls have suffered a setback. The US Supreme Court has ruled that judges need not issue injunctions in response to findings of patent infringement.

The ruling indicates that judges should weigh factors such as the public interest and a patent's "potential vagueness and suspect validity" when determining whether a product should be taken off the market. If ever a patent suffered "suspect validity," it seems to me to be the one at issue in this case, held by patent-holding company MercExchange and said to be infringed by eBay's "Buy It Now" feature.

RICK NELSON, CHIEF EDITOR

Unfortunately, eBay is not out of the woods. It must still contend with a jury's 2003 finding that eBay did infringe on MercExchange's patent. The case returns to lower courts for further litigation.

All this leads to the question of how qualified juries are to deal with technical patent issues. One proponent of juries is Rambus CEO Harold Hughes, who spoke with *Electronic Business* after Rambus's recent victory over Hynix in a patent dispute. (See the online version of this article for a link to the recorded interview, www.tmworld.com/2006_06.) He commented that key for him was the fact that, for the first time, Rambus was able to present its case to a jury, which accepted Rambus's contention that its patents were infringed.

Are juries qualified to evaluate patent claims?

Hynix takes a different view, issuing this statement to *Electronic News*: "While disappointed in the result, the focus of this phase of the trial was Rambus's patents, which were drafted to cover JEDEC standard SDR and DDR SDRAMs. The next phase will focus on Rambus's anticompetitive behavior in acquiring and enforcing these patents. In the next phase...Hynix seeks to have all of Rambus's patents in dispute held unenforceable."

The jury in the Rambus vs. Hynix case may have got it right. I've heard equally believable claims: that Rambus nefariously pirated and patented proposed JEDEC-standard technology, and that JEDEC members acquired Rambus technology under nondisclosure agreements and nefariously moved to embody that technology in JEDEC standards.

But based on jury decisions on other patent suits, including the one embroiling eBay, I have a hard time believing that having a jury on your side necessarily puts you on the side of the angels. T&MW

Last month, I commented on a dispute between D-Link and Poul-Henning Kamp, who maintains a time server. The dispute has been amicably resolved. Kamp will allow access to existing D-Link equipment; new D-Link products will not access Kamp's server. No other details were disclosed.

Post your comments at www.tmworld.com/blog.

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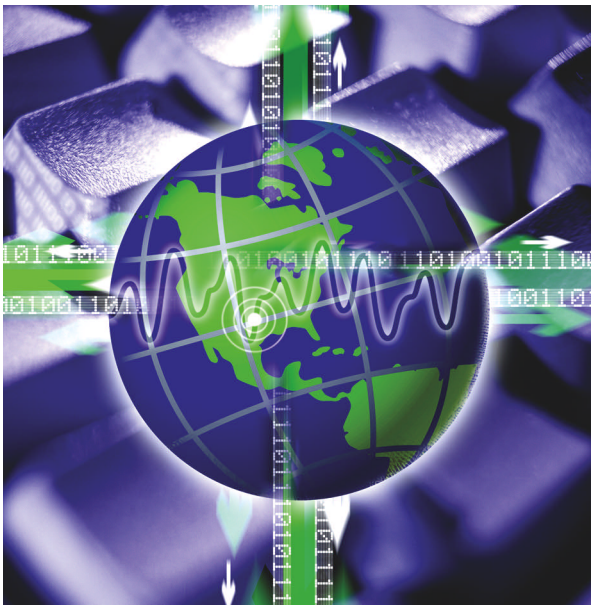
[An exclusive interview with a test engineer]



The underlying test code

Norman Kirchner recently joined Texas Instruments' Wireless Terminals Business Unit (Dallas, TX) as a software infrastructure engineer. He supports and writes infrastructure software that characterization engineers around the world use to evaluate new products utilizing LabView and TestStand. He has extensive LabView programming experience, having previously worked at Engineering Specialists (Brookfield, WI), a test-system integrator.

Q: How do you support characterization engineering?
A: Software engineers are an integral part of the characterization team. We write software that characterization engineers use to take measurements on ICs for wireless consumer products. The parts use a variety of technologies including Bluetooth, 3G cellular, and wireless LAN. The functions of those devices range from single-chip analog-to-digital converters (ADCs) to full-level SOCs. I work with TI engineers around the world to develop the software that will be used by a global characterization team.

Q: What's the procedure for developing code?
A: We work with design and characterization engineers to learn which measurements they need for a specific part. The characterization engineers take the part's specifications from design engineering and define the high-level measurements. Next, we look through a library of existing measurement routines and try to use prewritten and validated code wherever possible. We may also modify prewritten code and adapt it to a specific task.

The code modules do more than just control instruments and collect data. They perform data manipulation and post processing, producing measurements such as group delay and digital-to-analog-converter (DAC) linearity. Software engineers write code at their desktops and upload the software to a central source-code control server, making the new software available to test systems located around the world. We can remotely control any test system from our desks, so we can test the code on the system where it needs to run.

Q: How do you know if you have code that's appropriate to reuse in a test?
A: We keep a log of measurements taken by each code module. We also keep a list of supported instruments and the measurements they make. Experience helps in finding the best code module. We are looking toward automating the selection process to decrease the time and experience needed to design a test sequence.

Q: Do you write the entire test code, or does the characterization engineer get involved?
A: We write the software modules that make the measurements and compile the test results. We've also developed what we call "universal instruments." These are generic software modules for controlling generation and capturing instruments. A characterization engineer configures the universal instrument and it calls the underlying test code, which executes the necessary instrument drivers. The universal instrument software allows the measurement software to not care which instrument is behind it. Characterization engineers then use TestStand to define the sequence and configuration of the measurements.

Q: What challenges do you face in writing test code?
A: The biggest challenge is in designing software modules that fit a wide variety of requirements so we don't end up writing unique code for every part. For example, a module that calculates frequency response should work with a variety of instruments at frequencies from audio through R.F. T&MW

Every other month, we will publish an interview with an electronics engineer who has test, measurement, or inspection responsibilities. If you'd like to participate in a future column, contact Martin Rowe at mrowe@tmworld.com.

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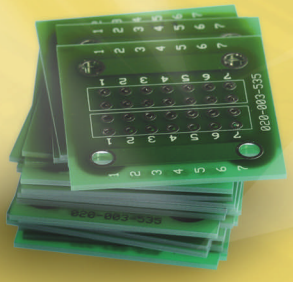

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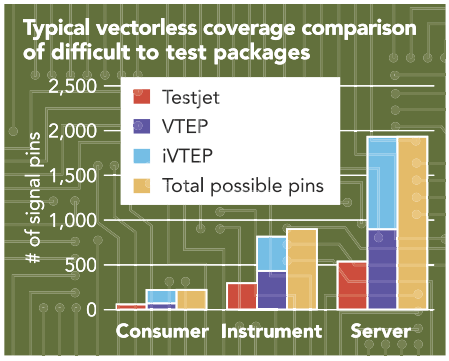

Agilent Technologies' Measurement Systems Division has extended the capabilities of its vectorless printed-circuit-board test technology with the release of Medalist iVTEP (intelligent Vectorless Test Extended Performance) software. The new iVTEP builds on vectorless test capabilities of the company's earlier VTEP and original TestJet technologies, which rely on package capacitance and tend to rely on the presence of substantial lead-frame metal.

N K Chari, Agilent in-circuit test marketing manager, explained that iVTEP targets micro-BGAs, flip chips, and other ultrasmall devices with minimal or no lead frames—all of which can exhibit insufficient capacitance to permit traditional vectorless approaches to work. Similarly, said Chris Jacobsen, Agilent R&D manager and technical marketing engineer, iVTEP targets devices whose attached heat spreaders introduce series capacitance, further limiting the effective capacitance available for traditional vectorless tests.

Jacobsen said that TestJet works above about 20 fF, VTEP works down to 5 fF (accommodating 1.27-mm-pitch BGAs), and iVTEP works well below 1 fF (accommodating 0.8-mm-pitch solder-ball packages). In an effort to protect Agilent's IP, Jacobsen would not say exactly what iVTEP measures—only that the measurement is less reliant on capacitance than were VTEP measurements. He did note that iVTEP is a software upgrade that works with any Agilent 3070PC or Medalist i5000 system equipped with a VTEP-compatible fixture. www.agilent.com/see/ICT.

GenICam releases slated for June

During The Vision Show East (see p. 15), the European Machine Vision Association (EMVA) announced that components of the new GenICam (GENeric programming Interface for CAMeras) standard are slated to be released in mid-June. Dr. Friedrich Dierks of Basler, who serves as secretary of the EMVA's GenICam standard group, announced that the GenApi applications programming interface will be released at a GenICam standard group meeting scheduled for June 12–15 in Montreal. At the same time, he said, the GenTL transport-layer protocol (for grabbing an image) will be issued in draft form.

The goal of GenICam is to provide a generic programming interface for all types of cameras, including ones employing GigE Vision, Camera Link, and IEEE 1394 interfaces. GenICam will specify a standard XML camera-description format that will make it easier for vendors of image-processing libraries to support diverse camera models.

From a customer viewpoint, Dierks said, GenICam will provide a standard user interface for configuring a camera, grabbing images, delivering events, and transferring image data. To comply with GenICam, camera vendors, he said, will provide a camera-description XML file that describes how camera functions map to specific camera registers or commands. Initially, seven of the 180 defined features are mandatory.

Dierks noted that the just-released GigE Vision standard mandates that GigE Vision cameras come with

Editors' CHOICE

LeCroy takes scope bandwidth lead

LeCroy's SDA 18000 serial data analyzer boasts a bandwidth of 18 GHz, and the company claims that it achieves the bandwidth without software enhancements. LeCroy also takes the single-channel sample rate lead at 60 Gsamples/s with this instrument. Waveform memory can reach 150 Msamples with a memory option.

To achieve the 18-GHz bandwidth, LeCroy uses a digital bandwidth interleave technique, which is based on RF heterodyne. The scope converts the incoming signal into two 6-GHz frequency bands for the 0–11 GHz range and one 8-GHz band for the 11 GHz to 18 GHz frequencies before digitizing the signal.

The SDA 18000 comes with LeCroy's Advanced Serial Data Analysis and Jitter software package (ASDA-J). Several options enhance the instruments for specific serial buses, including Serial ATA (SATA), Serial Attached SCSI (SAS), Fully Buffered DIMM (FB-DIMM), and PCI Express. LeCroy also offers a decoder package for 8b/10b encoded data streams. With this package, you select your data stream, and the SDA decodes the data and displays it with bus-specific commands.

Base price: $128,000. LeCroy has also introduced the 9-GHz SDA 9000, with prices starting at $90,000. *LeCroy, www.lecroy.com.*

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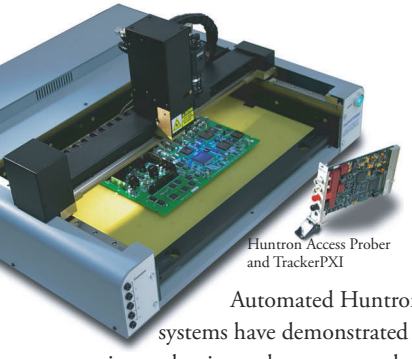

Huntron Access Prober and TrackerPXI

Automated Huntron systems have demonstrated test time reductions when compared to manual methods. Coupling automated probing with Huntron's new TrackerPXI and Workstation 4.0 software establishes a new standard for integrating power-off diagnostics into functional test platforms.

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GenICam-compliant files. Work is underway, he said, on requirements for IEEE 1394 cameras.

Dierks also noted that GenICam source code will be available to members of the GenICam group; runtime binaries sufficient for creating camera-description files will be available to others. The GenICam group has 10 members eligible to vote on the standard as well as 12 associate members. www.genicam.org.

Standards aim to reduce the risk of tin whiskers

JEDEC and International Electronics Manufacturing Initiative (iNEMI) have published two documents that should help manufacturers reduce the risk of tin whiskers in lead-free products. The first, JEDEC standard JESD201, "Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes," provides an environmental acceptance testing and reporting method for tin whisker susceptibility of tin and tin alloy surface finishes. The second document is a JEDEC/IPC joint publication, JP002, "Current Tin Whiskers Theory and Mitigation Practices Guideline." It describes theories about whisker formation and explains practices used to minimize whiskers. The documents can be downloaded from the JEDEC Web site. www.jedec.org.

CALENDAR

Semicon West, July 10–14, San Francisco, CA. Sponsored by SEMI. *www.semi.org.*

Design Automation Conference (DAC), July 24–28, San Francisco, CA. Sponsored by IEEE, SIGDA, EDA Consortium. *www.dac.com.*

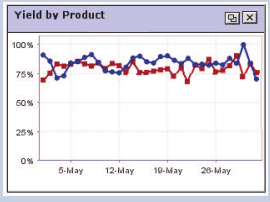
EMC Symposium, August 14–18, Portland, OR. Sponsored by IEEE, EMC Society. *www.emc2006.org.*

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

Editors' CHOICE

SigmaQuest addresses supplier quality

The Supplier Quality Insight application provides OEMs with the means to better manage and track the quality of suppliers' components. It's designed to foster a collaborative effort between suppliers and customers to ensure that suppliers meet target performance goals based on test data.



For companies employing Supplier Quality Insight, such data can be collected directly from suppliers' test equipment, pulled from data files, or loaded by suppliers into Web forms. An OEM customer can define a template indicating specification requirements. The data can span multiple real-time and historical data sources and encompass an entire extended supply chain, and it can also be integrated with data from design, ERP/MRP (enterprise resource planning/materials requirements planning), MES (manufacturing execution systems), and CRM (customer relationship management) applications.

The Supplier Quality Insight application can be accessed with any Web browser; it uses Internet standards such as SML (semantic markup language) and SOAP (Simple Object Access Protocol). It can also be deployed across multiple sites with differing computing infrastructures. The software is available for direct license or as a SigmaQuest Web-hosted software service. It's available as a stand-alone offering or as part of the SigmaSure product suite.

Base price: $35,000. *SigmaQuest, www.sigmaquest.com.*

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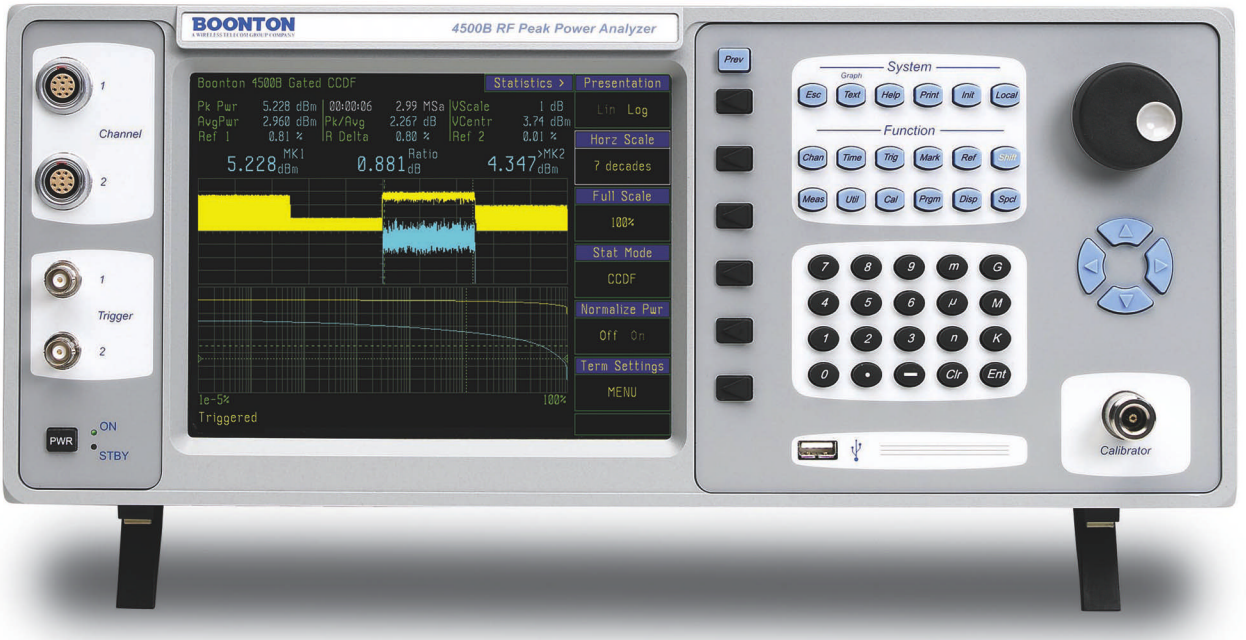

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Cameras, interfaces highlight vision gathering

> > > The Vision Show East, May 9–11, Boston, MA, Automated Imaging Association, www.machinevisiononline.org.

The GigE Vision standard formally debuted, and many exhibitors indicated support for the new spec. **Dalsa Coreco** (www.dalsa-coreco.com) demonstrated a 15-camera, four-computer GigE Vision application deployed throughout its booth. **National Instruments** (www.ni.com) announced it has added GigE Vision capability to its image-acquisition software. **Pleora Technologies** (www.pleora.com) demonstrated its iPORT AutoGEV software-mapping technology, which speeds compliance with the GigE Vision standard.

Interfaces such as FireWire, Camera Link, and USB also found support. Pleora's AutoGEV, for example, supports Camera Link cameras within GigE Vision applications. **Matrox Imaging** (www.matrox.com) announced a GigE Vision driver for the Matrox Imaging Library and also added an IEEE 1394b adapter card for its 4SightM vision computer. **Newnex Technology** (www.newnex.com) demonstrated optical repeaters that extend 800-Mbps FireWire over 10 km.

Several vendors aimed to speed image-processing tasks. **MathStar** (www.mathstar.com) introduced the Machine Vision Library for its Field Programmable Object Array (FPOA) devices. **Celoxica** (www.celoxica.com) highlighted its design tools for accelerating imaging algorithms on FPGAs. And Matrox debuted its FPGA developer's kit for programming FPGAs found on Matrox boards.

Among other board vendors, **Active Silicon** (www.activesilicon.com) demonstrated PCI Express frame grabbers, and **Euresys** (www.euresys.com) highlighted a PCI Express version of its video capture card. Demonstrating illumination products was **StockerYale** (www.stockeryale.com), which introduced its SpecBright line of LED modules, its Flat Top Generator laser-beam shaping module, and its Lasiris Slick laser. **Edmund Optics** (www.edmundoptics.com) previewed its EOS illumination technology, which combines fiber-optics with LED sources.

Camera exhibitors included **Toshiba Teli** (www.toshiba-teli.com), which showcased the CS6910G GigE Vision industrial camera. **Basler-VC** (www.basler-vc.com) introduced Scout cameras that come with GigE or FireWire interfaces and Pioneer cameras that come with GigE interfaces.

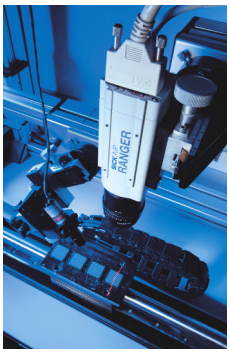
Imperx (www.imperx.com) introduced software utilities designed to provide extended access to its Lynx line of Camera Link and GigE cameras. **Sony** (www.sony.com/videocameras) introduced a version of its XCI-SX1 smart camera that's compatible with Windows XP Embedded. **PPT Vision** (www.pptvision.com) highlighted its Gigabit Ethernet Impact A-10 intelligent camera. **JAI Pulnix** (www.jaipulnix.com) displayed its GigE and dual-tap AccuPixel cameras.

Dage-MTI (www.dagemti.com) launched the XLM, an addition to its Excel line of FireWire cameras that offers a 2048x2048-pixel format based on **Kodak**'s (www.kodak.com/go/imagers) KAI-4021M progressive-scan sensor.

Allied Vision Technologies (www.alliedvisiontec.com) demonstrated its Guppy family, which offers a IEEE 1394a interface, and its Pike family, which offers an IEEE 1394b interface. **Point Grey Research** (www.ptgrey.com) debuted the Flea2 IEEE 1394b camera, which fits within a 29x29-30-mm housing, and the Firefly MV, which offers a 25x40-mm board-level footprint.

Adimec (www.adimec.com) announced its Adimec-4050m, a 4-Mpixel CMOS camera with Camera Link interface that delivers the image quality of CCD cameras. **Sick IVP** (www.sickivp.com) highlighted its Ranger C Camera Link model, which in 3-D mode can acquire up to 30,000 profiles per second.

Lumenera (www.lumenera.com) demonstrated its USB 2.0 digital cameras and announced that it has integrated its cameras with **MVTec** (www.mvtec.com) Halcon 7.1 software. **Videology** (www.videologyinc.com) featured its I-Net Stream Ethernet cameras and video servers and its USB 2.0 cameras and I/O boards. **Siemens** (www.siemens.com/simatic-sensors/mv) demonstrated products like its Simatic MV220 color area sensor. **Hamamatsu** (www.hamamatsu.com) highlighted its Microfocus x-ray sources and line-scan cameras. **Leutron Vision** (www.leutron.com) demonstrated its PicSight cameras, available with Camera Link, Ethernet, USB 2.0, and analog interfaces. Finally, **IMI Tech** (www.imi-tech.com) highlighted its line-up of FireWire, Camera Link, USB 2.0, and Ethernet cameras. T&MW



Ranger C performs the triangulation calculations necessary to develop 3-D coordinates. Courtesy of Sick IVP.

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RICK NELSON
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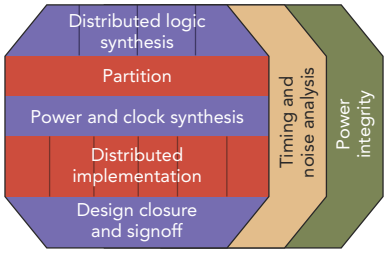
Integration paces point-tool development

A PANEL AT THE 2006 VLSI Test Symposium held May 1 in Berkeley, CA, explored the future of design for test (DFT). The primary question was whether point tools or integrated DFT environments are best, reports Ron Wilson, executive editor of our sibling publication *EDN* (Ref. 1). Panelists representing companies including Cadence Design Systems, Mentor Graphics, Synopsys, SynTest, and Virage Logic agreed that integration would be essential to link DFT with design tools, diagnostics tools, design-for-manufacture tools, and ATE.



Talus LX and PX, which target logic and physical design, respectively, combine to implement the functions shown here. Additional components will target design for manufacturability and yield learning. Courtesy of Magma Design Automation.

Wilson reports that panelist Sanjiv Taneja, VP for the Encounter Test product line at Cadence, commented that the EDA industry started as a collection of point tools that have evolved to fit within an all-encompassing architecture.

An all-encompassing architecture that addresses design, test, and yield is the goal of Magma Design Automation. The company targets the rapid design of ICs fabricated in 65-nm and smaller process geometries with its Talus platform, which the company describes as a lithography-aware implementation flow from RTL to tape-out. Now in beta release, Talus addresses timing, area, power, signal integrity, DFT, and manufacturability, according to Behrooz Zahiri, a senior marketing director at Magma.

When I asked Zahiri about the technology, he told me that increased automation is one of the key features of Talus. He described previous EDA methods as "electronic design assistance," with significant scripting and other efforts required to tie together DFT, built-in self-test (BIST), wireload modeling, floor planning, and a host of other functions that might exist as point tools. Such manual approaches become untenable, he said, as investments rise from $5 million per design at 130 nm to potentially $50 million or more at 45 nm.

Zahiri said that initially, Talus is available in two versions: Talus LX and PX, which target logic and physical design, respectively. Additional enhancements, he said, will target manufacturability and yield learning. More details, he said, will be available at the Design Automation conference (July 24–28, San Francisco, CA).

But despite efforts to combine design, test, and yield functions into a single flow, alternatives continue to emerge. For example, Stratosphere Solutions has just debuted its StratoPro platform, which, according to Prashant Maniar, chief strategy officer, is part of an effort to "build differentiated technology that meets a focused market demand"—in this case, alleviating yield fallout caused by parametric variability. And Incentia Design Systems recently released a new version of its TimeCraft software, designed to improve the accuracy and efficiency of static timing analysis for 90- and 65-nm designs.

Ultimately, the trend toward integration is inexorable, but so is the emergence of new tools that address problems occurring on leading-edge processes. T&MW

REFERENCE

1. Wilson, Ron, "Panel probes future of design-for-test," *EDN*, May 3, 2006. www.edn.com/article/ca6331013.

11.5-GHz QFN socket

Ironwood Electronics has introduced a QFN (quad flat-pack no-lead) socket for 0.4-mm-pitch devices. The SS-QFN104A-01 operates to 11.5 GHz with less than 1-dB of insertion loss. Designed for up to 500,000 actuation cycles, the socket can dissipate 7 W from –40 to +120°C without the need for an additional heat sink. It accommodates a chip with 104 pins plus ground pad. Current-carrying capacity is 1.5 A per pin. Actuation force is 20 g per pin. Base price: $1480. www.ironwoodelectronics.com

Pin Scale HX supports 12.8 Gbps

Agilent Technologies has announced the Agilent Pin Scale HX high-speed extension card for its 93000 SOC Series tester. The new card supports characterization for devices and interfaces with data rates up to 12.8 Gbps. The Pin Scale HX is designed to provide the signal integrity required for at-speed design characterization and production test of Serdes device interfaces such as PCI Express and HyperTransport. www.agilent.com.

European lab buys Sapphire D-10

Credence Systems has announced that Microtec, an independent, certified European test lab, has purchased multiple Sapphire D-10 ATE systems. The lab will use the systems to test digital and mixed-signal devices intended for multimedia audio and video as well as industrial applications. www.credence.com, www.microtec.de.

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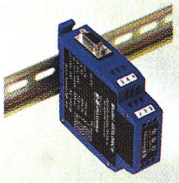

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- Auto MDI-X for hassle free cabling
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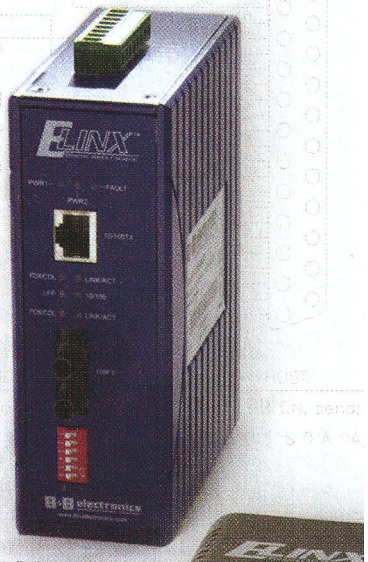
- DIP switch configuration for
  - Link-fault-pass-through (enabled or disabled)
  - 10/100 Mbps data rates (auto or forced modes)
  - Full or half-duplex (auto or forced modes)

Additional features of the Industrial EIR Series

- Rugged DIN mount metal case
- Wide -34 to 74 C temp range
- Redundant 10 - 48 VDC power inputs
- Alarm relay output

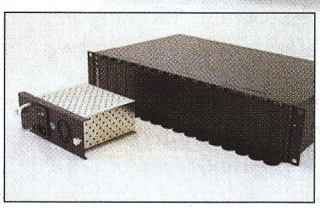


EIR Ethernet Media Converter

EIS Ethernet Media Converter

Industrial Series Model No.	Description	Fiber Port	Price
EIR-M-ST	Multi-mode	ST	$229.95
EIR-M-SC	Multi-mode	SC	$229.95
EIR-S-SC	Single-mode	SC	$389.95

Commercial Series Model No.	Description	Fiber Port	Price
EIS-M-ST	Multi-mode	ST	$129.95
EIS-M-SC	Multi-mode	SC	$129.95
EIS-S-SC	Single-mode	SC	$289.95



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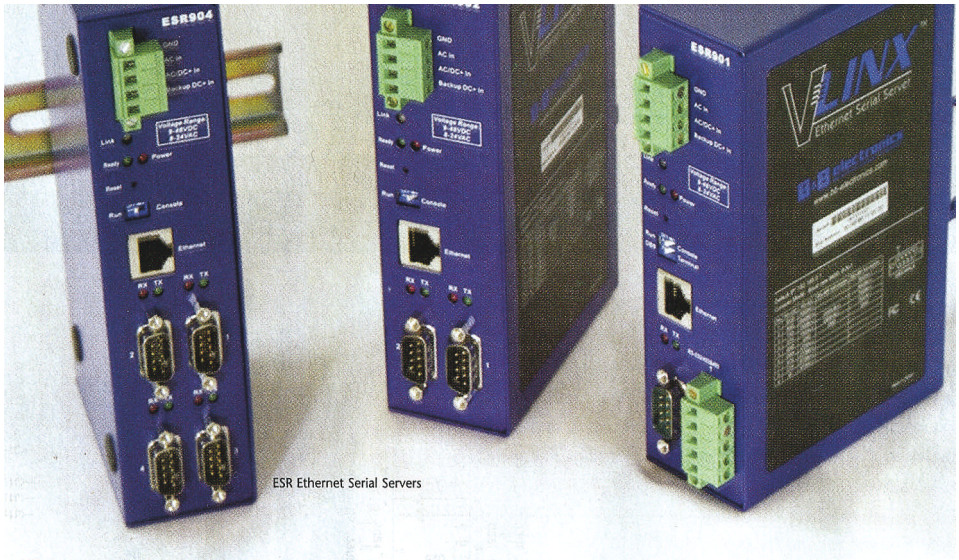


ESR Ethernet Serial Servers

If it has a serial port and you have an Ethernet LAN, you can connect with Vlinx Serial Servers. Your legacy equipment will communicate over the LAN just as if it was directly connected to your PC. Use your existing application software without leaving your desk. Even connect from outside your LAN via the internet. Vlinx Serial Servers are available in Industrial and Commercial versions to best fit your application.

ESR Series Industrial Ethernet Serial Servers

The Vlinx ESR Series Industrial Ethernet Serial Servers are built for use in tough environments. The rugged metal cases are IP30 and DIN rail mountable. They operate on a wide range of AC or DC voltages and support redundant DC power.

ESR Series Industrial Serial Server Features

- Supports TCP server, TCP client, UDP, paired and virtual COM modes
- Low latency performance
- Auto detecting 10/100 Ethernet port
- Ports software selectable RS-232, RS-422 or RS-485
- Easy setup and management with web and telnet consoles
- LED indicators provide at-a-glance status
- Wide operating temperature: -10°C to 80°C
- Dimensions: ESR901/902 1.75 x 6.1 x 4.1 in. ESR904 1.75 x 7.1 x 4.1 in.
- Slim-profile DIN rail mounting
- Wide range power input: 9 VDC to 48 VDC or 8 VAC to 24VAC
- Redundant DC power input for failsafe operation
- Compatible with POTS, cellular, and satellite modems

Model No.	Description	Price
ESR901	1-Port RS-232/422/485	$199.95
ESR902	2-Port RS-232/422/485	$299.95
ESR904	4-Port RS-232/422/485	$499.95

Ethernet to Serial

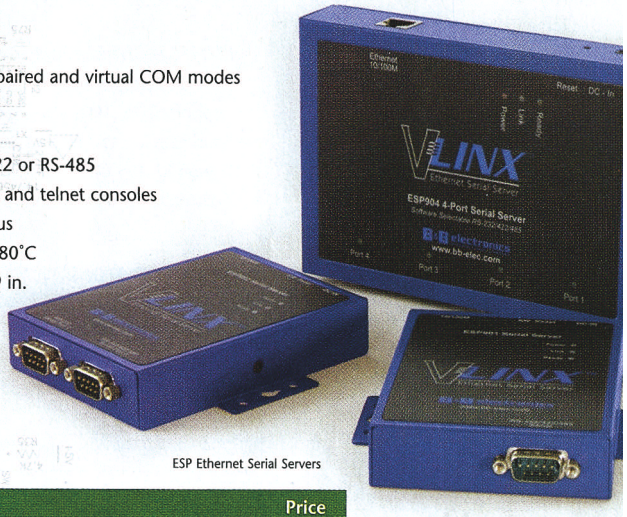
Ethernet enable serial ports on industrial equipment

ESP Series Ethernet Serial Servers

The Vlinx ESP Series Ethernet Serial Servers are ideal for demanding commercial applications such as retail point-of-sale, fuel stations and hospitality. Vlinx servers offer the same great communications features as the industrial ESR line, but with mounting and power options optimum for commercial installations.

ESP Series Serial Server Features

- Supports TCP server, TCP client, UDP, paired and virtual COM modes
- Low latency performance
- Auto detecting 10/100 Ethernet port
- Ports software selectable RS-232, RS-422 or RS-485
- Easy setup and management with web and telnet consoles
- LED indicators provide at-a-glance status
- Wide operating temperature: -10°C to 80°C
- Dimensions: ESP901/902 3.4 x 4.5 x .9 in.
  ESP904 7.3 x 4.2 x 1.1 in.
- Rugged panel mount case
- Power Input: 12 VDC power jack, power supply included
- Compatible with POTS, cellular, and satellite modems



ESP Ethernet Serial Servers

Model No.	Description	Price
ESP901	Single-port RS-232/422/485	$149.95
ESP902	One RS-232/422/485 port, one RS-232 port	$199.95
ESP904	4-port RS-232/422/485	$399.95
ES1A	Serial/Ethernet LAN converter	$129.95

Space a problem?

This ultra compact Ethernet serial converter fits almost anywhere. Model ES1A is powered by 5 VDC power supply. (included)

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USB

Industrial Converters & Isolators

Connect your PC or laptop's USB port to any RS-232, RS-422 or RS-485 port with B&B Electronics USB to Serial Converters. Windows automatically configures the output as an additional COM port, compatible with your Windows application. 2000 VDC optical isolation protects your PC or laptop from dangerous surges, spikes and ground loops.

Features

- 2000 VDC optical isolation
- LEDs for transmit and receive lines
- Automatic configuration on Windows 98, ME, 2000 and XP
- No power supply required
- Includes 1 meter USB cable

RS-232 USB/serial converter unique features

- Full handshake support (TD, RD, RTS, CTS, DTR, DSR, DCD, RI, GND)
- DB9 male (DTE)
- Baud rates up to 460 Kbps

RS-422/485 USB/serial converter unique features

- Covered terminal blocks
- Supports TDA, TDB, RDA, RDB, GND
- Baud rates up to 115.2 Kbps
- Use on RS-485 2-wire or RS-422/485 4-wire networks
- Automatic Send Data Control (for hassle free RS-485 compatibility)

Model No.	Description	Price
USO9ML2	USB to isolated RS-232 converter	$139.95
USOTL4	USB to isolated RS-422/485 converter	$139.95
USTL4	Non-isolated USB to RS-422/485 converter	$119.95

USB to Serial Converters

Ideal for field service applications!

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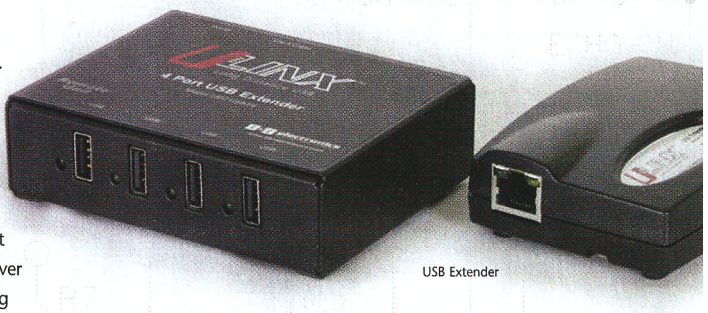
Communicate USB Data up to 500 meters (1640 feet) "legally" The USB standard calls for a maximum range of 5 meters. Ulinx Extenders increase USB up to 100 meters with standard Cat5 cabling, and up to 500 meters with fiber optic cabling.

Ulinx Extenders are fully compliant with the USB specification and deliver all of the benefits of USB, including remote device powering and plug-and-play operation. Complete with power supplies and 1 meter USB cable when required. User provides Category 5 and fiber optic cables for all models except UEF10M which includes an attached 10m fiber cable.



USB Extender

NEW low price!

Features

- Extend USB up to 500 meters over fiber
- Extend USB up to 100 meters over Cat5 copper
- Fully compliant with the USB standard
- Available for USB 1.1 or 2.0
- 4 USB ports on UEC100M/4, UEF500M/4

Model No.	USB Type	Extension Media /Dist.	USB Ports	Power Suppy	USB Hub Support	Unique Features	Price
UEC50M	1.1	Copper/50 m (164 ft)	1	None (bus powered)	Distance tradeoff	No power supply required	$89.95
UEC100M/4	1.1	Copper/100 m (330 ft)	4	Included	Yes	4 USB ports	$329.95
U2EC50M	2.0	Copper/50 m (164 ft)	1	Included (qty 2)	Yes	480 Mbps	$549.95
UEF10M	1.1	Fiber /10 m (33 ft)	1	Included	Yes	Isolated	$199.95
UEF500M/4	1.1	Fiber/500 m (1640 ft)	4	Included (qty 2)	Yes	Longest distance	$699.95
ANYWHEREUSB/5	1.1	Ethernet IP/Unlimited	5	Included	Yes	USB over IP	$262.95

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Industrial Converters & Isolators

Convert RS-232 signals to RS-422 or RS-485

Convert, Protect and Extend RS-232/422/485

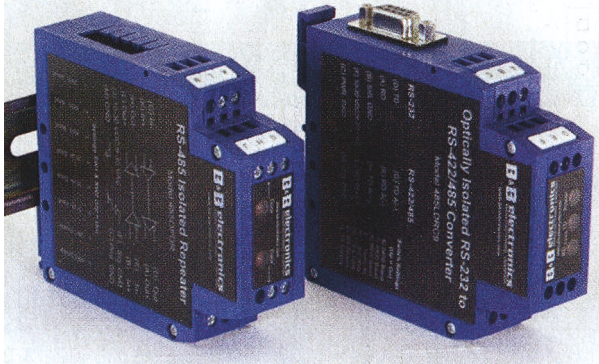
Extend serial communications up to 4,000 feet with these Industrial Serial Converters and Isolators. Wide temp and voltage range inputs and slim-line DIN rail mounting make these converters a perfect fit in any industrial installation.

Optical isolation protects your devices from surges and ground loops. Each converter includes 2000 volts of optical isolation to protect your equipment from these electrical hazards.

Common Features

- Multidrop to up to 32 nodes
- Increase communication range up to 4,000 feet
- Wide temperature range (-40° to 80° C)
- Wide power range (10 to 30 VDC)
- MODBUS compatible
- DIN rail mount
- 2000 V optical isolation; built-in RS-485 surge protection

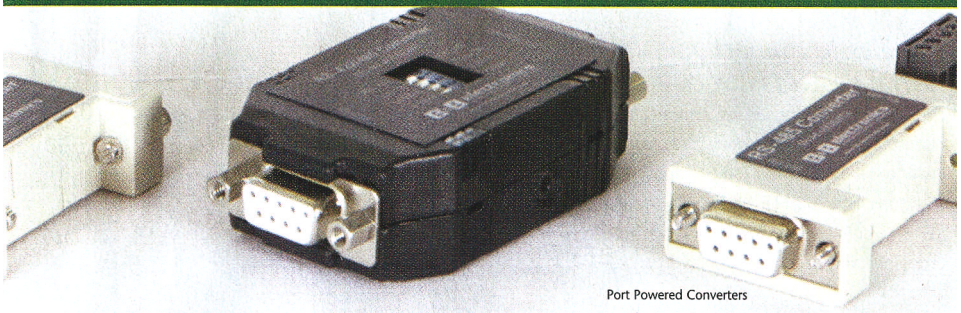
Model No.	Description	Price
485LDRC9	RS-232 to RS-485 DIN rail mount converter	$139.95
485OPDR	RS-422/485 optically isolated repeater	$154.95
232OPDR	RS-232 optically isolated repeater	$154.95
PS5R-A12	DIN rail power supply12 VDC @ 600 mA	$44.95
DR-30-12	DIN rail power supply 12 VDC @ 2 A	$47.00



Industrial Converters & Isolators

Port Powered Converters

Convert RS-232 to RS-485 with no power supply



Port Powered Converters

These port-powered converters change TD and RD RS-232 lines to RS-485 signals. All are port powered and feature Automatic Send Data Control. (SDC)

SDC automatically enables the RS-485 driver when data is present on the RS-232 side. Control of the driver is automatic at rates up to 115.2 kbps.

Features

- Powered from RS-232 handshake lines - no power supply needed!
- Extend RS-232 signals to 4,000 feet (1.2 km)
- Automatic Send Data Control - no software drivers needed!
- Communicate at baud rates to 115.2 kbps
- Alternate power supply methods shown below

Order Today!

Model No.	RS-232 Connector	RS-485 Connector	Power Supply	Output	Price
485SD9R	DB9 female	DB9 female	Port powered	2-wire RS-485	$74.95
485SD9TB	DB9 female	Terminal block	Port powered (or 485PS2)	2-wire RS-485	$74.95
4WSD9R	DB9 female	DB9 female	Port powered (or 485PS)	4-wire RS-422 (2-wire or 4-wire RS-485)	$79.95

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Wireless

Wirelessly connect your legacy serial devices

Wirelessly connect your legacy serial devices with 802.11

The Vlinx™ family of wireless Ethernet Serial Servers transparently connects, configures, and communicates with serial devices over industry leading 802.11g 54Mbps, and 802.11b 11Mbps compatible WiFi wireless connections. For applications where running cable is not an option.

Space a problem?

This ultra compact Ethernet serial converter fits almost anywhere. Model ES1AWB is powered by a 5 VDC power supply (included).

Features

- High performance up to 54 Mbps 802.11g connectivity
- Wirelessly connect legacy serial devices to your LAN
- Ease of installation and setup via integrated web server
- Remote device monitoring and diagnostics
- Ideal for applications requiring virtual COM ports, serial tunneling, TCP socket, or UDP socket
- Rugged, IP30 enclosure, DIN, or panel mount options
- Omni Directional, revers SMA antenna included

ESR901W232 Wireless Serial Server

ES1AWB Wireless Serial Server

Order One Today!

Model No.	Description	802.11	Price
ESR901W232	Single-port RS-232 DB9	g/b	$349.95
ESR901W485	Single-port RS-422/485, terminal block	g/b	$349.95
ESR902W	Dual-port DB9: one RS-232 only; one RS-232/422/485	g/b	$449.95
ESR904W	4-Port DB9: two RS-232, Two RS-232/422/485	g/b	$649.95
ES1AWB	Wireless Serial/Ethernet LAN converter	b	$249.95

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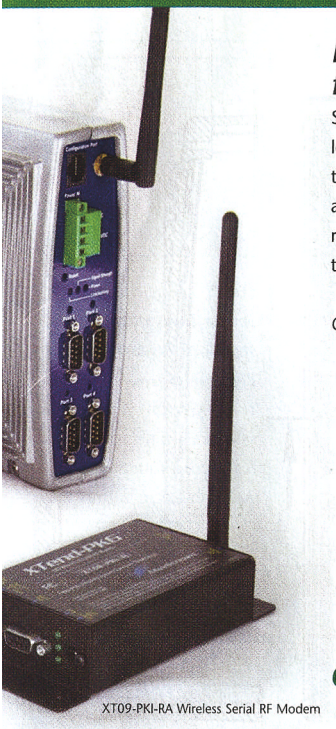

XT09-PKI-RA Wireless Serial RF Modem

MaxStream Proprietary RF wireless radio for long and short range communications

Some data communications applications defy cabling. Whether you're facing long distances, impossible cable routing, or frequent relocation of devices, the simplicity, functionality, and reliability of these wireless solutions is the answer. These radio modems are easy to install and transparent to use. This range and reliability, offered at a lower price, set these modems apart from their competition.

Common features

- Operation modes: Peer-to-peer, point to multi-point, point-to-point, multi-drop transparent network, MODBUS
- Configuration: AT command line, Windows software
- Spread Spectrum: FHSS (Frequency Hopping Spread Spectrum)
- Frequency: ISM Band, 902 to 928 MHz or 2.400 to 2.4385 GHz
- Modulation: FSK (Frequency Shift Keying)
- Antenna: Reverse polarity SMA 2.1 dB 1/2 wave dipole (included with packaged radios unless otherwise specified)
- Mounting: Panel mountable (OEM solutions use a pin header and standoffs)
- Power supply: Included (OEM modules do not include a power supply)

Order Today!

Family	Transmit Throughput	Power	0 to 70 C Model No.	Price	-40 to 85 C Model	Price
9XTend	115 Kbps	1 mW to 1 W			XT09-PKI-RA	$299.95
9XStream	9600 bps	100 mW	X09-009PKC-RA	$249.95	X09-009PKI-RA	$264.95
24XStream	9600 bps	50 mW	X24-009PKC-RA	$199.95	X24-009PKI-RA	$213.95
XPress	935 Kbps	125 mW	XEB09-C (pair of two)	$698.95	XEB09-I (pair of two)	$998.95

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All Terminal Blocks are not alike!

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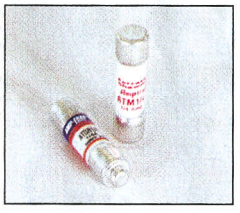
Feed through • Feed through terminal blocks allow one-to-one connections.

Multi-level • Multi level terminal blocks offer 2 and 3 times the wiring of a standard feed through terminal block on same DIN space.

Ground • Ground terminal blocks mechanically and electrically link wires to the DIN rail by using a metal clamping bar.

Disconnects • B&B Electronics offer an abundance of disconnects in an array of capacities to fit your needs.

Fuse holders • For all of your fuse needs, from Class CC, midget, 5 x 20 mm, and 1 1/4" x 1/4"



Fuses

Ferraz Shawmut world standard fuses at B&B Electronics prices

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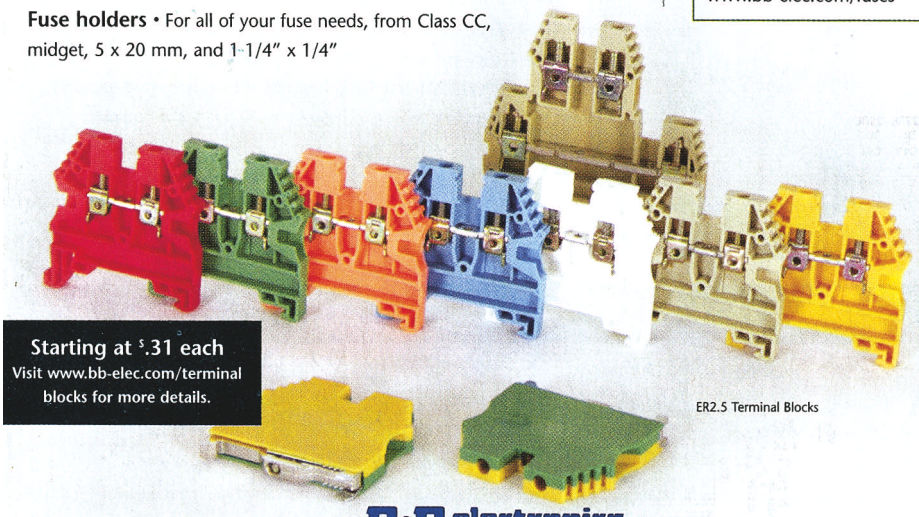

ER2.5 Terminal Blocks

Starting at $.31 each

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Relays

These relays are powerful, flexible, expandable, and effective

Programmable Relays

Programmable Relays

B&B Electronics selected SG2 series offers the price of a programmable relay with the capability of a small PLC. It comes with Free software that will empower you with its simplicity offering ladder logic programming, function block programming and simulation and testing.

In addition to these programmable relays we carry Electromechanical/Solid State Relays. Visit www.bb-elec.com/relays for more information on these great products.

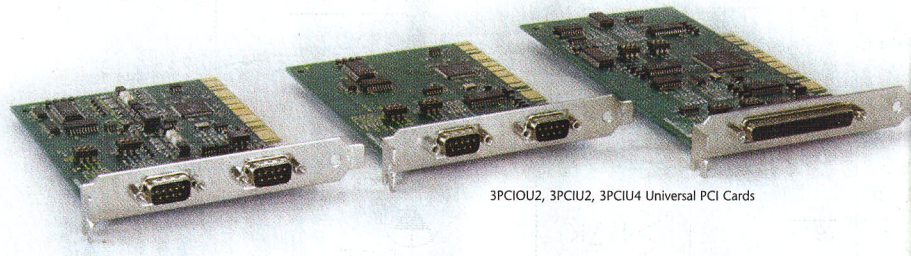
Programmable Relays

Model No.	AC Power 100~240	DC Power DC 24V	Discrete Inputs	Analog Inputs	Relay Outputs	Real Time Clock	LCD Display	Keypad	1KHz Input	Price
SG2-10HR-A	Yes		6		4	Yes	Yes	Yes		$102.50
SG2-12HR-D		Yes	6	2	4	Yes	Yes	Yes	Yes	$99.00
SG2-20VR-D		Yes	8	4	0	Yes	Yes	Yes	No	$149.00

Multi-Interface Universal PCI Cards

One to eight port RS-232/422/485 cards - standard and optically isolated models

Universal PCI cards suit most any application. Output can be RS-232, RS-422, or RS-485. Use RS-422 to extend range, RS-485 to extend range and provide multi-drop ability.



3PCIOU2, 3PCIU2, 3PCIU4 Universal PCI Cards

Features

- Available in 1, 2, 4 or 8 ports
- Optically isolated and standard models
- Multi-interface: RS-232/422/485 selectable
- 5 V and 3.3 V PCI bus compatible
- PCI-X compatible
- Positive-connecting DB9M ports

Isolated models Model No.	Ports	Interface	Connector	Price
3PCIOU1	1	RS-232/422/485	DB9 male	$199.95
3PCIOU2	2	RS-232/422/485	DB9 male	$289.95
3PCIOU4	4	2 Ports RS-232/422/485 2 Ports RS-422/485	2x DB9 male on card 2x DB9 male use 2nd expansion slot (ribbon cables and bracket included)	$449.95

Non-isolated models Model No.	Ports	Interface	Connector	Price
3PCIU2	2	RS-232/422/485	DB9 male	$179.95
3PCIU4	4	RS-232/422/485	DB37 female (includes DB37 to 4x DB9 male cable)	$239.95
3PCIU8	8	4 Ports RS-232/422/485 4 Ports RS-232	DB78 female (includes DB78 to 8x DB9 male cable)	$399.95

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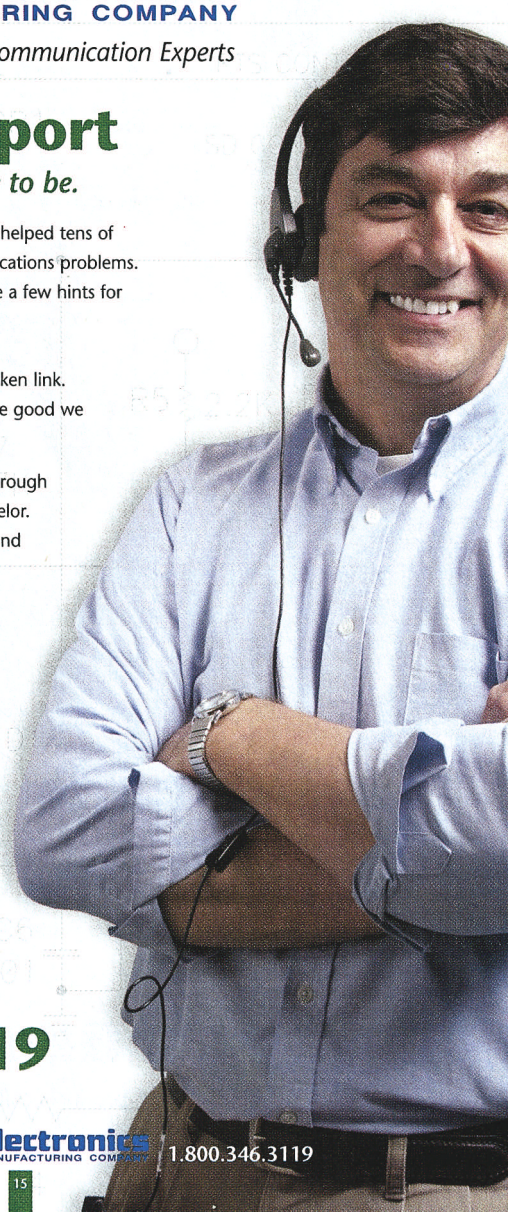
The B&B Electronics Technical Support Team has helped tens of thousands of customers with their data communications problems. In that time, we've learned a few things and have a few hints for our existing and new customers.

- Don't waste hours testing and retesting a broken link. Give us a call. We're here to help. Chances are good we can save you both time and stress.
- Sometimes it just helps to talk your system through with someone. Consider us your camp counselor. Give us a call. We'll talk the system through and figure it out together.
- If you think you're going to use time-on-hold to read a manual or get another cup of coffee, think again. B&B Electronics customers don't get put on hold (well, almost never anyway).



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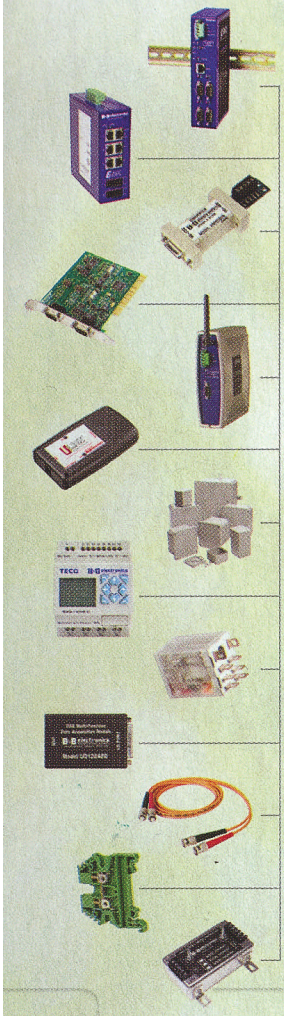

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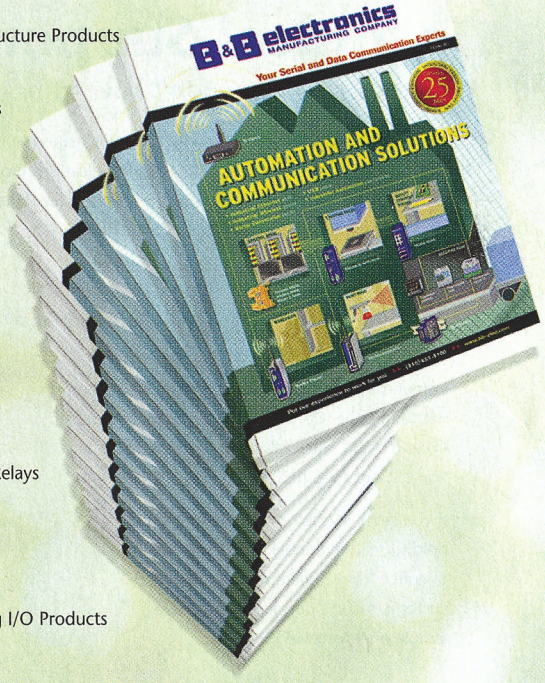

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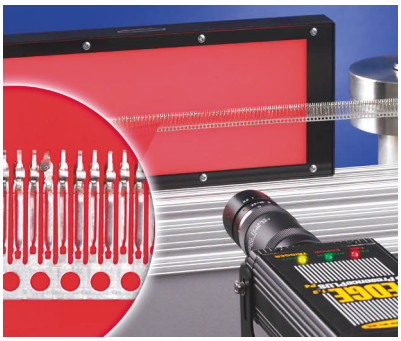
JON TITUS
CONTRIBUTING TECHNICAL EDITOR
jontitus@comcast.net

Sensors simplify vision systems

MANY ENGINEERS think a vision system requires a big budget and a lot of headaches to get cameras, lights, and software working together. Powerful microprocessors and dense memory chips now let vendors offer small, inexpensive vision sensors that handle sophisticated inspection tasks with ease. These sensors can take over for older, expensive equipment that requires regular maintenance and programming.

In addition, small inexpensive sensors let engineers add inspection equipment to a production line where high costs previously prevented its use.



The PresencePLUS P4 Edge 1.3 sensor from Banner Engineering provides a 1280x1024-pixel image detector that lets the unit capture many regions of interest. Internal memory saves as many as 12 inspection "recipes" for different products. Courtesy of Banner Engineering.

Adding inspection stations along a production line helps catch defects quickly and prevents defective products from going through additional processing steps. Rejects get swept off a line—and accounted for—as soon as sensors detect them.

Companies such as Cognex and Banner Engineering offer a variety of vision sensors that vary in their capabilities. Buyers can choose simple absence/presence detectors or sophisticated vision systems that match geometrical patterns and detect image features. Sensor prices start in the $1000 to $2000 range.

Vision sensors provide a graphical user interface (GUI) that lets you enter information about what you want to inspect and the features you want to look for on an object. A laptop computer, connected through an Ethernet cable, serves as a GUI display and data-entry terminal. A vision sensor requires no knowledge of machine-vision algorithms.

For the most part, sensor "learning" involves the capture of one or more images of known-good products as well as products that get close to the known-bad category. Then, you identify regions of interest.

"Say you must inspect a cell-phone keypad," said Jeff Schmitz, corporate business manager for vision sensors at Banner Engineering. "You'd image a known 'good' cell keypad, and draw a boundary around the keys you wish to verify. Then, the software will match the image of each keypad inspected with the stored pattern to give a percent match."

Vision sensors make pass/fail decisions and generate an output that causes immediate action. But they also can communicate with other equipment.

"The DVT sensors offer communication tools," said Conner Henry, product marketing manager for the DVT product line at Cognex. "Those tools control the Ethernet port to communicate with most devices—from programmable logic controllers to robots—that use a standard protocol. A uniform series of setup steps for each protocol makes it easy for new users to communicate vision information to other equipment."

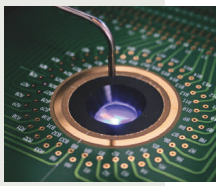
An Ethernet port also lets vision sensors communicate with a host computer that can pass inspection results to statistical process-control software available from third parties. And some sensor networks let you simultaneously monitor the images from each connected sensor. These products prove good things really do come in small packages. T&MW

JEOL untethers TEM

JEOL USA has demonstrated wireless remote-control capability for its transmission electron microscopes. The wireless remote-control functionality builds on a wired TEM remote-control capability the company introduced last summer with its Sirius TEM enhancement, designed to let you "see atoms from 6000 miles away," as Dr. Mike Kresker, JEOL USA VP and product manager, put it in a press release issued at the time. Sirius consists of a knob set that, in the wireless implementation, connects to a laptop that's in turn outfitted with a cellular communications card. www.jeolusa.com.

BlueRay gets automated

Suss MicroTec reports that its semiautomatic BlueRay prober can be field-upgraded to a fully automatic configuration within a couple of hours. An upgraded BlueRay can provide the electrical and optical measurement capabilities necessary to test any optoelectronic, MEMS, or RF device with throughput of up to 70,000 dies per hour. www.suss.com/blueray.



Sherlock 7 debuts

The ipd group of Dalsa has announced the release of its Sherlock 7 machine-vision software. Sherlock 7 adds support for color image processing to features such as positioning, measuring, analysis, and identification tools. For customers with proprietary processing requirements, Sherlock 7 supports the inclusion of custom algorithms that can be directly plugged into the design environment. www.goipd.com.

Device programming perfected.

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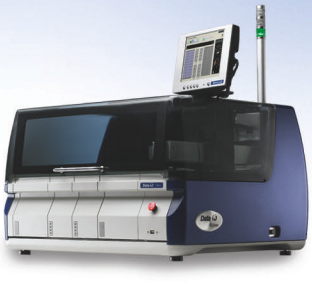

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COMMUNICATIONS TEST

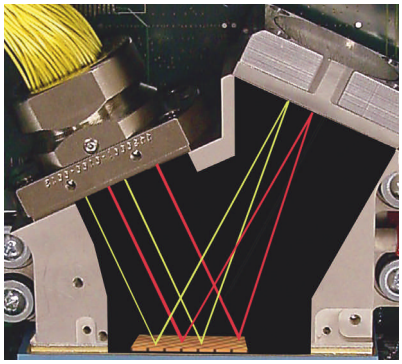
The network *is* the test bed

Scientists often need to correlate massive amounts of data located at different sites, and today's networks are beginning to accommodate this need. One example is the OptIPuter project (www.optiputer.net), a collaborative research project of the University of California San Diego (UCSD), the University of Illinois Chicago (UIC), and others that was built to show that today's technology can handle the task.

The backbone of the OptIPuter is a 10-Gbps optical network that can dynamically allocate bandwidth as needed, which lets the OptIPuter put unused resources to work handling data-intensive applications such as life science, earth science, microscopy, and imaging. Because network engineers at participating sites are free to expand or reconfigure their network nodes (each site, or "cluster," may contain several hundred nodes), the testing of the network never stops.

Computing and network researchers have developed custom software that automatically assigns bandwidth where needed. Part of the bandwidth allocation comes at the physical layer, where optical switches from Glimmerglass and Calient let engineers reconfigure the network to accommodate changing bandwidth demands.

"Because it's a research project, the network is in fact a test bed," said OptIPuter chief infrastructure officer Greg Hidley at UCSD. "Every time someone reconfigures or adds to the network, we have to test that it can still allocate bandwidth as needed." Testing involves measuring the throughput at the application layer with network software, but Hidley and others can also perform lower-layer tests such as packet monitoring and optical power measurements. The online version of this article contains a link to a diagram of the UCSD OptIPuter network (www.tmworld.com/2006_06).



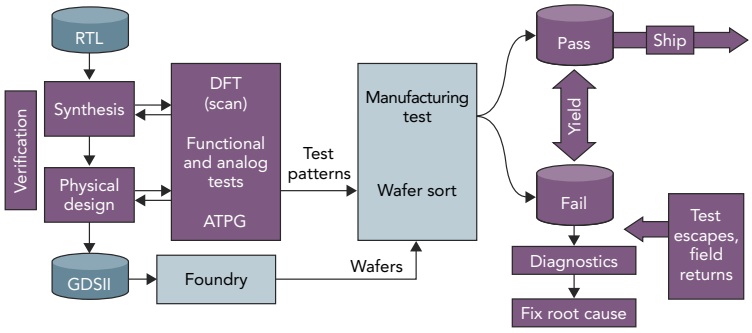
Optical switches let researchers reconfigure the OptIPuter network under software control. Courtesy of Glimmerglass.

Martin Rowe, Senior Technical Editor

SEMICONDUCTOR TEST

Test's role on the path to zero-defect devices

The effectiveness of semiconductor manufacturing test has a direct impact on the quality of shipped silicon and on the economical efficiency of the overall test cost in the supply chain. Typically, suppliers and customers have negotiated agreements on acceptable defects per million (DPM) levels that represent an optimum tradeoff between test coverage and cost. Applications in the medical, automotive, and aerospace fields, however, have quality requirements that supersede supply-chain optimization considerations. In these environments, achieving "zero defects" is the objective and the main challenge.



The zero-defect manufacturing test ecosystem extends from design and verification through wafer sort and manufacturing test and on to diagnostics.

In many applications requiring zero defects, engineers traditionally focused on testing analog circuits and on addressing overall reliability. Vendors and customers did not have to devote expensive resources to testing digital components, because the digital content was small, and digital devices were predictable in terms of their defect behavior.

Today, however, the digital content of zero-defect applications is increasing significantly, and designs are migrating to 90-, 65-, and even 45-nm technology nodes. At these advanced nodes, defect behavior of digital circuitry is far less predictable using traditional fault models. Today's designs continue to require the traditional structural-test techniques, but they also require specialized fault modeling and test procedures to detect the subtle timing defects that can appear in nanometer designs.

Successful zero-defect designs require a full-chip test infrastructure; the ability to perform stuck-at, at-speed, and faster-than-at-speed tests; and tests that target defect-based fault models, all in an architecture that supports test cost management by using on-chip compression. In addition, process improvement requires

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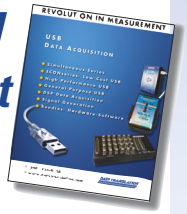

DATA TRANSLATION®

Test's role on the path to zero-defect devices *(continued)*

volume diagnostics that can identify yield limiters as well as precision diagnostics to locate root failures. To read more about meeting the individual challenges of digital zero-defect testing and to learn details of approaches to dealing with these challenges, see the online version of this article at www.tmworld.com/2006_06.

Mick Tegethoff and Vivek Chickermani, Cadence Design Systems

BOOK REVIEW

A semiconductor test primer

VLSI Test Principles and Architectures: Design for Testability, Laung-Terng Wang, Chen-Wen Wu, and Xiaoquing Wen (editors), Elsevier Science (www.books.elsevier.com), 2006. 706 pages (prepublication review copy). $49.95.

This massive compendium (706 pages in manuscript form in the version I reviewed) of semiconductor test information is intended to serve as a textbook, but it is also a thorough reference that deserves space on the engineer's shelf. Twenty-seven contributors represent both academia and industry. Editors and contributors Chen-Wen Wu and Xiaoquing Wen represent, respectively, National Tsing Wa University and Kyushu Institute of Technology, while LT Wang is founder, president, and CEO of SynTest.

Representatives of Cisco Systems, Cadence Design Systems, Wavecrest, Intel, LogicVision, Mentor Graphics, and SynTest represent EDA toolmakers and semiconductor designers and manufacturers, yet they refrain from giving the hard sell on any particular products. One of the few sections to mention specific EDA products is a chapter on test compression, and the editors provide a balanced look at multiple vendors' offerings. A section on RAM BIST compilers notes that commercial implementations are available, but it confines its description to an academic version. The book, expected to ship June 30, will come with a CD containing SynTest software.

Chapter 1 defines some basic test terms. You can skip this section, but if you're unclear on the distinction between fault and failure, for instance, you may want to give it a look. To demonstrate that the authors aren't restricting their efforts to chip test, the opening chapter introduces board test and boundary-scan technology as well.

Chapter 2 delves into design-for-testability, covering controllability and observability and various types of scan cells. Chapters 3, 4, and 5 build on this information, covering logic and fault simulation, test generation, and BIST. Chapter 6 introduces test compression and includes comments on five vendors' products. Chapter 7 rounds out the broad discussion of testability by covering logic diagnosis and its application to design debug, failure analysis, and yield ramp-up.

You can choose among subsequent chapters based on your area of interest. Chapters 8 and 9 address memory test and repair. Chapter 10 goes into detail on boundary-scan and core-based testing, covering the IEEE 1149 dot-4 and dot-6 extensions for AC-interconnect and analog test as well as the IEEE 1500 standard for SOC core test. Chapter 11 covers analog and mixed-signal test. The concluding chapter looks at the emerging problems facing scan and BIST as process geometries shrink below 65 nm.

Much of the information here could be gleaned from industry white papers and from perusing years and years of ITC and VLSI Test Symposium proceedings, but this book is a valuable collection of relevant material in a convenient package.

For a longer review of this book, see the online version of this article, www.tmworld.com/2006_06. Disclaimer: Elsevier Science is a subsidiary of *Test & Measurement World*'s parent company.

Rick Nelson, Chief Editor

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RF/MICROWAVE

See the unseen

DEVICE UNDER TEST

A radar and vision system that provides views of landing sites that the naked eye can't see. The system helps pilots land in rain, snow, dust, smoke, and other adverse weather conditions. An embedded image processor fuses images from the radar and camera with still photos of a landing site to form real-time moving images that help pilots land safely.

THE CHALLENGE

Integrate and test a system consisting of an embedded controller, a millimeter-wave (94-GHz) radar, infrared cameras, and a flat-panel display. Test the ability of system components to communicate with the controller. Simulate a landing in order to perform system-level tests in the lab before deploying the system into an aircraft.

THE TOOLS

- Agilent Technologies: spectrum analyzer. www.tm.agilent.com.
- MathWorks: simulation software. www.mathworks.com.
- Tektronix: logic analyzer and oscilloscope. www.tektronix.com.
- VMetro: PCI bus analyzer, data recorder. www.vmetro.com.

PROJECT DESCRIPTION

BAE Systems (Los Angeles, CA) has developed a vision system (**figure**) that helps pilots land in zero-ceiling and zero-visibility conditions. The system uses radar, two video cameras, and three infrared cameras to "see" where a pilot can't. An embedded processor with industrial-grade PCI video cards processes images, and the system contains a database of still images from landing sites. By scrolling through the images of a landing site, the processor forms a moving map. The processor fuses images from the radar sensor, vision cameras, and infrared cameras to produce images on the map that the pilot uses to land an aircraft.

Three infrared cameras provide left, center, and right views from the cockpit. To accurately process the camera and radar images into a single image, the processor collects data on the aircraft's location, altitude, and pitch; the radar antenna position; and the position of where the pilot is looking.

In order to test the system prior to deployment in a test aircraft, the BAE engineers needed to integrate the system components and write image-processing code. First, they had to verify that video cards would properly operate in the image processor. A PCI bus analyzer and a logic analyzer monitored and captured bus activity between the cards and the embedded CPU. A spectrum analyzer verified that the radar was working by measuring the frequency and amplitude of signals from objects at known distances from the radar antenna.

Once engineers integrated the system, they performed lab tests. At first, they pointed the cameras at objects located known distances from the cameras and radar antenna. When they were convinced that the system could fuse the video images into a single image, they tried using it to capture moving objects. They pointed the cameras out the window of their lab and took images of automobile traffic.

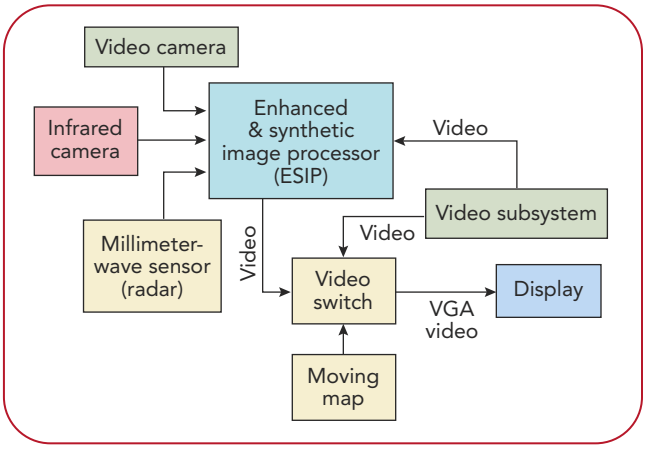
After debugging their own embedded code and verifying data integrity, the BAE engineers were ready for a flight test. They installed the system into a Boeing 757 at NASA Langley Research Center (Ref 1). Flight tests proved that the system was ready for larger deployment.

LESSONS LEARNED

"We had difficulty getting some of the components to work because they lacked Linux drivers," said senior hardware engineer Don Brown. "We had to work side by side with card manufacturers to get drivers that worked because some of the drivers they developed for us had code bugs."

"We assumed that each component would work right out of the box," added senior software engineer Ben Montalvo. "But we had to qualify each component to give us confidence in our data. We also should have verified our data by simulating the sensor outputs with Matlab scripts before relying on a functional test. We also should have integrated our data recorder into the overall system earlier than we did. Doing so would have let us more easily verify the integrity of our data before switching to the code used in the image processor."

Martin Rowe, Senior Technical Editor.



An embedded controller receives video images from cameras and from a radar system, then fuses them with still images to produce a visual representation of a landing site. Courtesy of BAE Systems.

REFERENCE

1. Hughes, David, "MMW Ready To Roll," *Aviation Week*, November 28, 2005. www.baesystems-ps.com/capabilities/daynightallweather/1-13660246%20Eprint.pdf.

The WORLD IS STILL ANALOG

MARTIN ROWE, SENIOR TECHNICAL EDITOR

Engineers at Analog Devices put amplifiers, converters, and RF devices through rigorous tests so that consumer and industrial products will work properly.

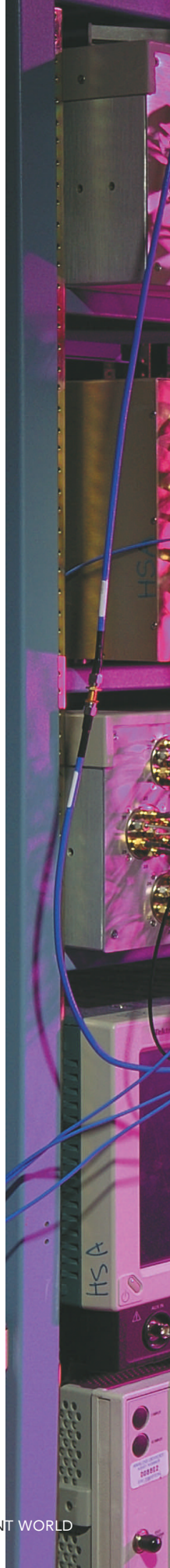
WILMINGTON, MA—Many people say, "It's a digital world," but don't say that to engineers at Analog Devices. At the company's facility here, engineers test preproduction ICs that handle analog signal processing in cell phones, base stations, audio equipment, instrumentation, and many other "digital" products.

The Wilmington facility includes a complete wafer-fab line that produces engineering prototypes and production wafers. The assembly of engineering ICs takes place in Wilmington or at a third-party contractor's facility. Production wafers are assembled at other facilities around the world.

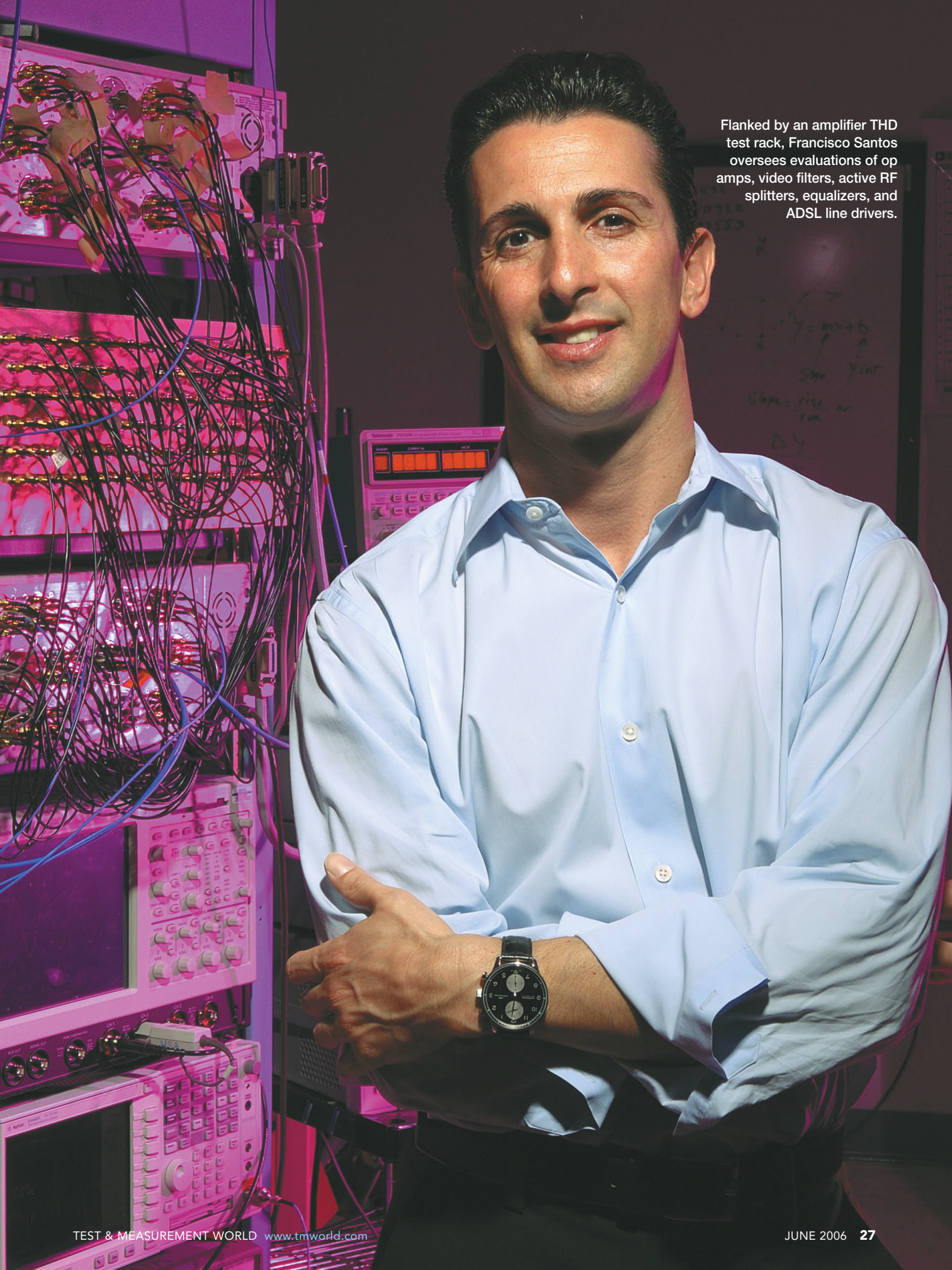
Before an op amp, digital-to-analog converter (DAC), analog-to-digital converter (ADC), audio coder/decoder (CODEC), or RF IC is ready for production, it must endure weeks of tests by product engineers. These engineers test devices for every specification that's intended for a data sheet, and they also perform other tests they deem necessary. Test results often become the "typical" performance characteristics published in data sheets. Upon completing an evaluation, product engineers write a 30-to-40-page test report. (My first job after college was as a product engineer at Analog Devices. The online version of this article contains a summary of my experience, www.tmworld.com/2006_06.)

Each preproduction IC needs an evaluation board that provides engineers with access to signal pins and programming registers. Boards often contain communication ports such as USB to communicate with a PC. A product engineer is responsible for developing an evaluation board. During my visit to Wilmington, I heard a common refrain about performing a product evaluation: "Is it the board or is it the device under test that's causing the problem?" Often, the engineers must go through a process of elimination to locate a problem's source.

When they initially test a product, the engineers measure the DUT with manually controlled bench instruments. Once they're convinced that the part functions properly, they often run automated tests with in-house test software on the bench or connect the evaluation boards to automated test racks. Finally, they use production ATE systems to perform tests on devices over a range of temperatures and power-supply voltages. The ATE systems are built by a former division of Analog Devices. The company now focuses entirely on the design and manufacture of ICs.



MARK WILSON



Flanked by an amplifier THD test rack, Francisco Santos oversees evaluations of op amps, video filters, active RF splitters, equalizers, and ADSL line drivers.

Op amps, splitters, filters, and more

Francisco Santos is the product development engineering manager for the high-speed amplifier group. His team of engineers evaluates products such as high-speed, low-distortion amplifiers, video filters, active RF splitters, cable drivers, equalizers, and ADSL line drivers.

Engineers in Santos' group evaluated the AD8099, a low-noise, low-distortion, high-speed op amp that has a gain-bandwidth product of 3.8 GHz. Because Analog Devices develops numerous amplifiers each year, engineers have built several automated test systems for the engineering lab. One of these systems measures total-harmonic distortion (THD), an important specification for op amps. "Distortion levels for our low-distortion op amps can run 140 dB below the fundamental frequency of a test signal," said Santos, "so the noise floor of our instruments is very important. We don't want to be measuring the noise in the instrument."

When performed manually, harmonic-distortion measurements can take weeks, but engineers such as Greg DiSanto now run the test in just hours with an automated test station in the lab (**Figure 1**). DiSanto characterizes THD versus frequency, amplitude, supply voltage, and common-mode voltage. This station uses a Stanford Research signal source to produce test frequencies up to 200 kHz and a Rohde & Schwarz unit at higher frequencies. When used to characterize video amplifiers, both signal sources produce 2-V_{p-p} sine waves set to the 3-dB point of the selected low-pass filter. Low-pass filters from Allen Avionics—connected through 18-GHz RF switches from Keithley Instruments—remove harmonics before they reach the DUT. More RF switches connect the DUT's output to filters, which enables an Agilent Technologies spectrum analyzer to measure distortion caused by second and third harmonics.

MARK WILSON

Product engineer Gina Colangelo evaluates high-speed DACs prior to production.

The engineers also adjust the DC offset of the input signal, looking for the point where clipping causes distortion. "Open loop gain loss causes distortion," said Santos. "We adjust the input signal's bias level until we find a voltage that saturates the op amp's output stage."

Engineers in Santos' group also evaluate active video splitters such as the ADA4302-4 1:4 splitter. Product engineer Frank Ciarlone's automated test station (**Figure 2**) measures composite second-order (CSO) distortion, composite triple-beat (CTB) distortion, and cross-modulation (XMOD) distortion. The signal generator, built by Matrix Test Equipment, contains an array of frequency sources producing 135 distinct sine waves with frequencies from 55.25 MHz to 865.25 MHz. The engineers terminate one output with a 75-Ω load and connect the other output to a programmable band-stop filter. A 75-Ω-to-50-Ω wideband, low-insertion-loss transformer is used to match the input impedance of a Rohde & Schwarz spectrum analyzer.

To characterize CSO and CTB, Ciarlone measures intermodulation products generated by the 135 channels. The band-stop filter on the DUT's output removes

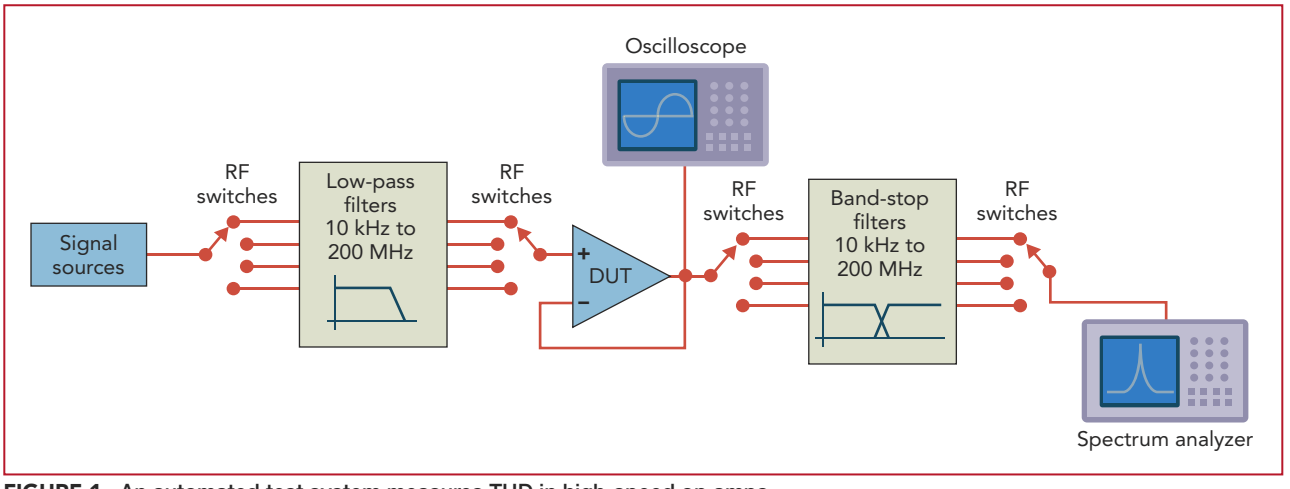


FIGURE 1. An automated test system measures THD in high-speed op amps.

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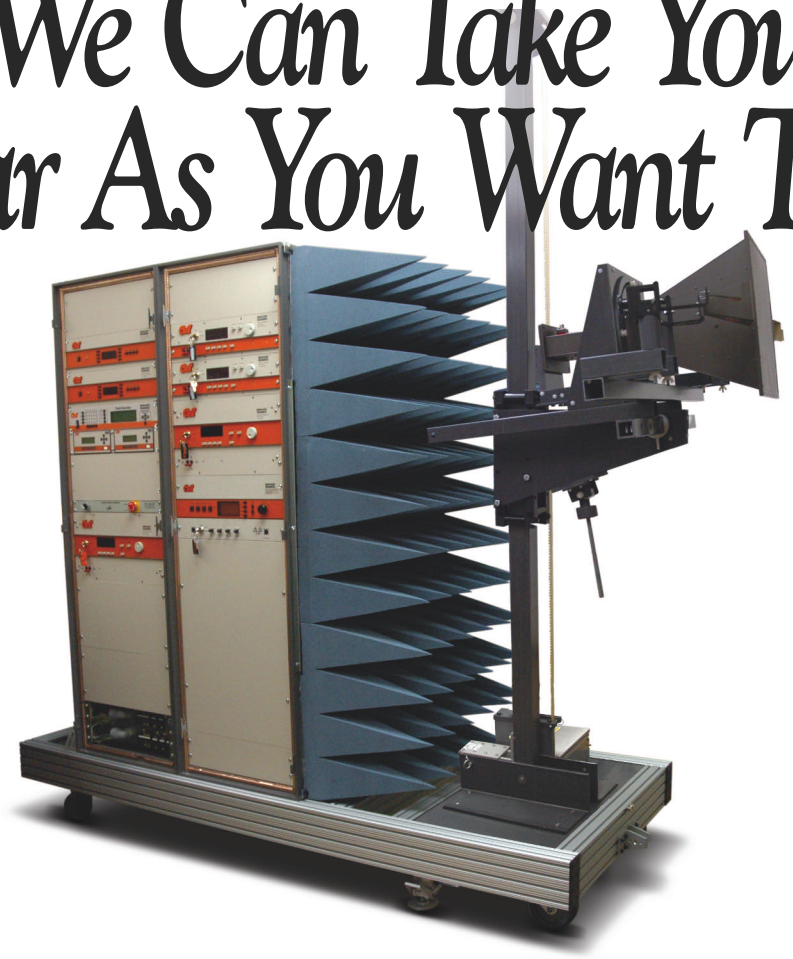

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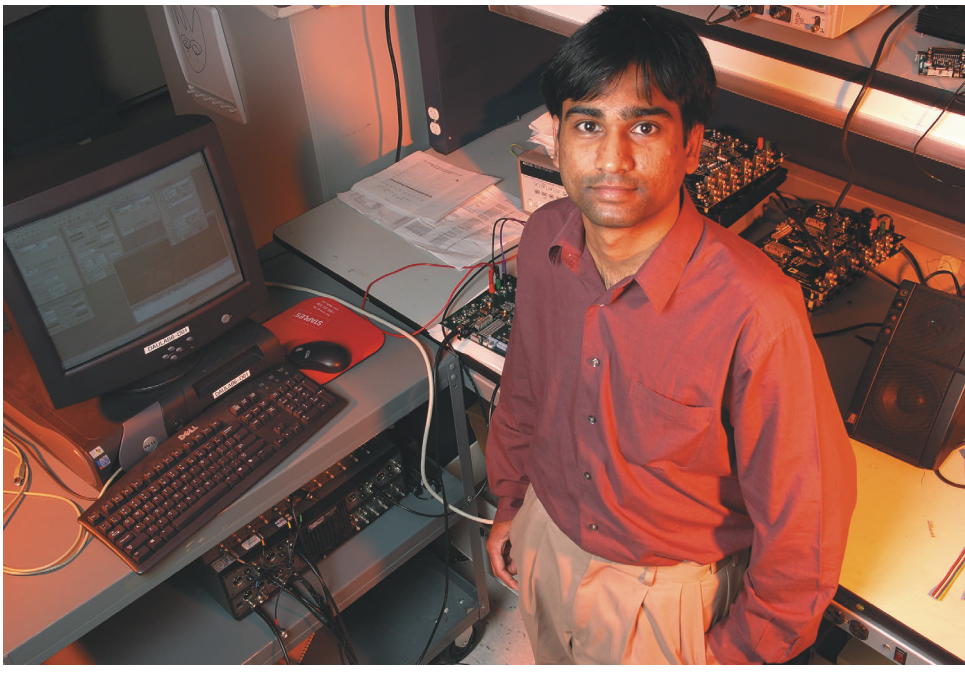
out-of-band carriers. He measures XMOD by modulating all channels except the one of interest and measuring the resulting "spill over" in the unmodulated channel band. "We can get the data we need in a fraction of the time with all channels on," noted Ciarlone, "and fully evaluate a splitter."

Engineers in the high-speed amplifier group use Agilent Vee to control both the THD and splitter testers. They have automated several other measurements such as noise-spectral density using spectrum analyzers from Agilent and Rohde & Schwarz, and video-filter frequency response and group delay with an Agilent network analyzer and Keithley RF switch.



Product engineer Chirag Patel evaluates audio CODECs for use in automotive sound systems.

MARK WILSON

DACs and ADCs

Well known for its DACs and ADCs, Analog Devices makes components that go into cellular handsets and base stations, instrumentation equipment, and embedded systems. Product engineers Justin Munson and Gina Colangelo test high-speed DACs. Munson focuses on parts that use LVDS digital inputs while Colangelo focuses on DACs that use single-ended, CMOS digital inputs.

Munson's most recently released product is the AD9736, a 1.2-Gsample/s, 14-bit DAC. He's currently evaluating a higher-speed part. He measures noise spectral density (NSD), THD, spurious-free dynamic range (SFDR), intermodulation distortion (IMD), adjacent-channel power, bit-to-bit skews, linearity, and power consumption. Test signals include a single-tone and dual-tone sine wave. An Agilent ParBERT generates the signals in digital form, and it provides 14 pairs of differential signals.

When he evaluated the AD9736, Munson tested the devices at 600 Msamples/s, 800 Msamples/s, 1 Gsample/s, and 1.2 Gsamples/s. At 1 Gsample/s, Munson programs the ParBERT to sweep from DC to 490 MHz, just under the Nyquist frequency of 500 MHz.

"When you evaluate DACs that run at speeds over 1 Gsample/s," said Munson, "the layout of your evaluation board is critical. It's often difficult to isolate problems that come from the board or from the device under test. An evaluation board requires good power-supply decoupling, and its digital traces need to be separated from analog traces."

DACs such as the AD9736 have differential analog outputs, which minimize system errors caused by ground loops. That's fine for engineers who design the devices into systems, but it makes testing more difficult than with single-ended outputs. Munson uses transformer loads instead of amplifier loads in his evaluations.

"Transformer loads make it easier to evaluate a DAC because they convert differential outputs to single-ended outputs without having to worry about the additional nonlinearities of an amplifier output stage," he said. Munson found that he needs more than one transformer to fully test a DAC because of the operating bandwidth limitations of each transformer.

For her part, Colangelo evaluates DACs such as the AD9779, which use single-ended CMOS inputs. She performs the same measurements as Munson. "Some customers are not yet comfortable with the high-speed LVDS interface DACs so they choose a CMOS interface DAC with added digital functionality," she said. The input data rate can run at speeds up to 300 Msamples/s. To generate the single-ended test signals,

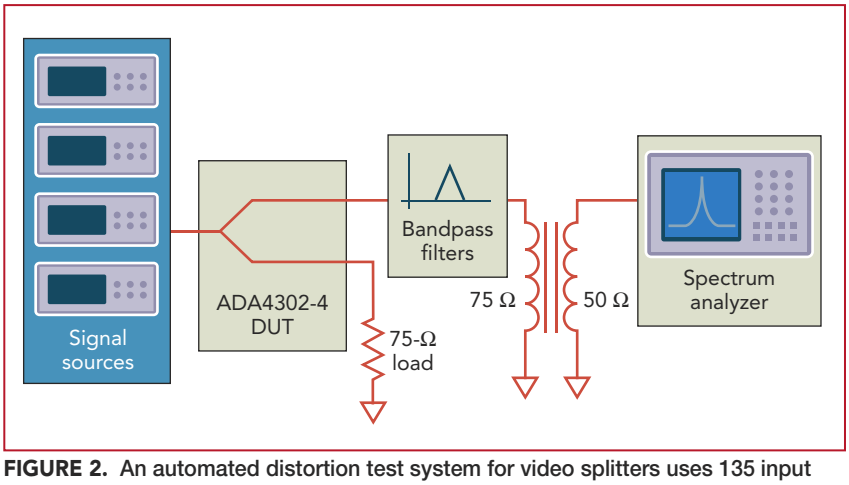


FIGURE 2. An automated distortion test system for video splitters uses 135 input signals.

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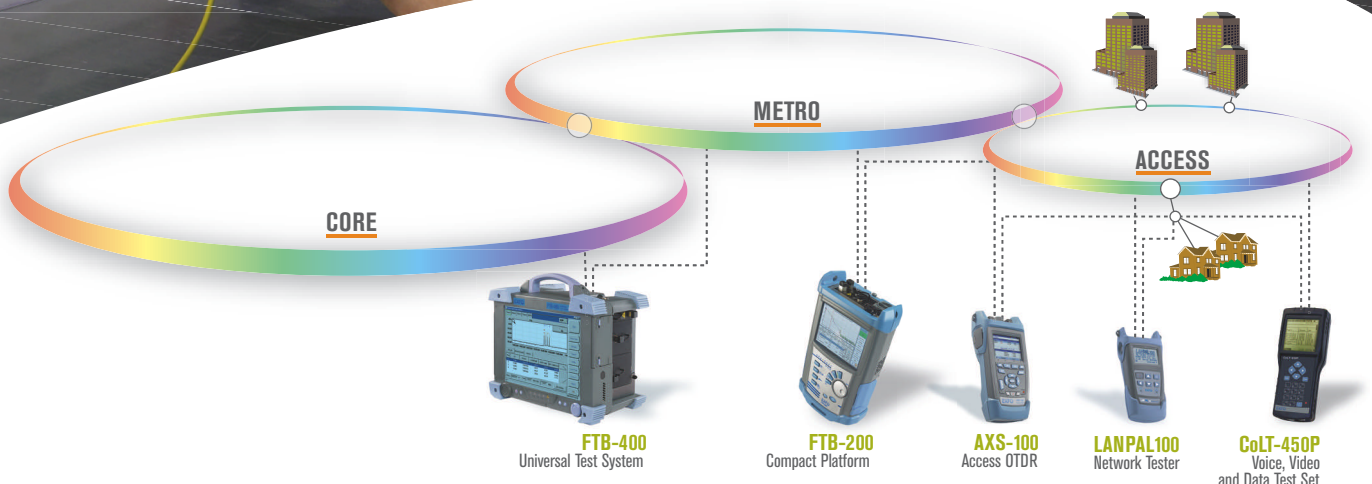

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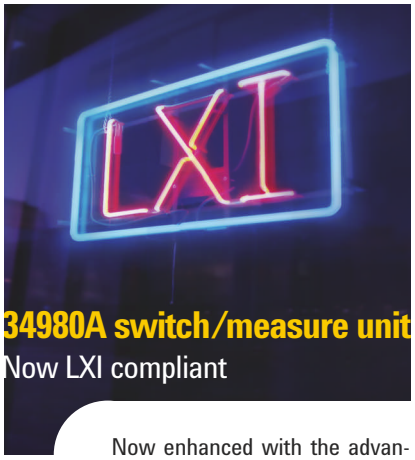

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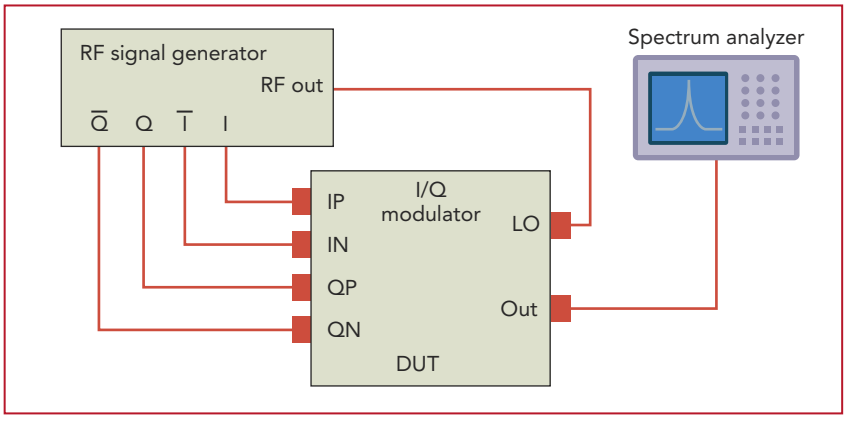

FIGURE 3. The spectrum analyzer measures noise, adjacent channel leakage ratio (ACLR), and sidebands in an I/Q modulator.

Colangelo uses a pattern generator developed at Analog Devices.

Used primarily in cellular base stations, the AD9779 contains two DACs to generate I/Q modulated signals. Users can power down parts of the device to conserve power. For example, they can power down the DAC cores when a handset isn't transmitting.

The AD9779 uses digital filters to smooth the device's analog output. The digital filters require their own clocks, but those clocks can add distortion to a DAC's analog output. Isolating clocks from analog circuits is a challenge for both IC designers and product engineers. "We have to test not only the device," said Colangelo, "but the evaluation board, too. If you power down the DAC section of a device but leave the digital control section powered and measure its output with a spectrum analyzer, you shouldn't see any spurious signals. If you do, you may have a board issue."

When they initially evaluate a DAC, Munson and Colangelo perform bench tests manually. "We need to first understand how the device works," said Colangelo. "After that, we can automate our testing. We must also make sure that the spectrum analyzer isn't adding distortion to our measurements." To get the best possible performance, they use two spectrum analyzers to evaluate their DACs. "We use a Rohde & Schwarz spectrum analyzer up to 100 MHz," noted Colangelo. "Above 100 MHz, we switch to an Agilent instrument."

After Munson and Colangelo are confident that the part works and that their evaluations don't add distortion, they run a series of automated measurements. They control the pattern generator and spectrum analyzers using software writ-

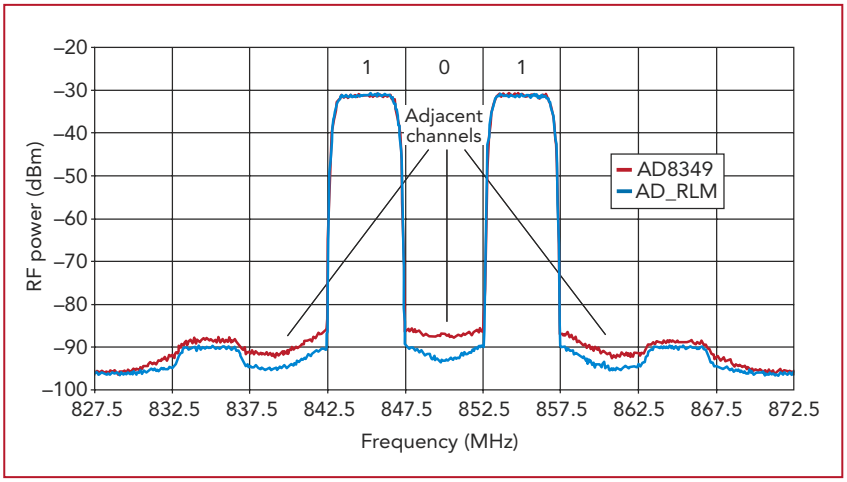

FIGURE 4. An adjacent channel leakage measurement shows less adjacent and alternant-channel noise in the newer part (blue trace).

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ten in National Instruments' LabView. Following bench tests, Munson and Colangelo will use an ATE system to make many of the same measurements over a range of temperature and power-supply voltages.

ADCs are another core product for Analog Devices, and product engineer Chris Carney evaluates them. He tests ADCs that use both differential LVDS and single-ended CMOS digital outputs.

"Typically, 350 Msamples/s is the switchover point from CMOS to LVDS," said Carney, "but some customers want LVDS outputs even at lower speeds." Customers who use ADCs at speeds of 100 Msamples/s to 200 Msamples/s may prefer LVDS because the differential outputs use a smaller voltage swing.

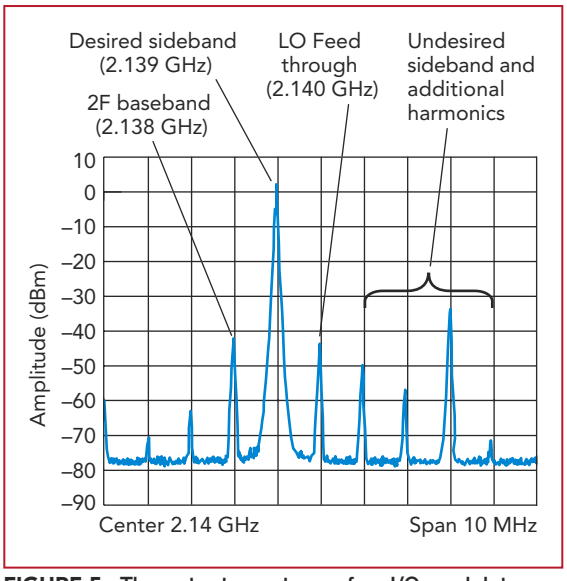

FIGURE 5. The output spectrum of an I/O modulator shows undesired frequency components.

Carney's ADC evaluation boards connect to a FIFO memory board. Two versions, with 16 kbytes and 32 kbytes of memory, let him run an ADC at full speed and analyze the data offline after transferring the data to a PC. Like Munson and Colangelo, Carney begins his evaluations running manual tests on the bench before automating his measurements.

His FIFO board works with in-house ADC test software called LabAlyzer, which is an executable written in LabView. With LabAlyzer, Carney can configure an ADC, capture data, and perform FFTs to measure distortion and integral nonlinearity. One of his tasks is to control a register that adjusts the ADC's input bias voltage. Once he finds the optimal bias voltage, design engineers can set that voltage in silicon for production devices.

Audio CODECs

Analog Devices also manufactures a line of audio ICs that contain DACs, ADCs, sample-rate converters, and digital-signal processors that run several audio algorithms. Under the direction of digital audio products engineering manager Steven Roy, product engineer Chirag Patel evaluates audio CODECs. His latest is the AD1938, designed for automotive sound systems. It contains four stereo DACs and two stereo ADCs. The device is an upgrade to the AD1836A, which has three stereo DACs and two stereo ADCs. New cars have sound systems with eight speakers and they need four stereo DACs.

Starting with an evaluation board, Patel configures the CODEC for a specific mode of operation. He configures the sample rate, serial data format, and volume by writing to registers through a serial peripheral interface (SPI) port. The device has 18 user registers and several others for in-house diagnostics only. The evaluation board communicates with a PC through a USB port.

When first debugging a new part, Patel runs into some of the same issues as his colleagues Munson and Colangelo—identifying the source of noise. "It's a process of elimination," noted Patel. "If I see noise on the power-supply lines, I use an external power supply instead of the evaluation board's supply."

Patel measures IMD, THD+noise, linearity, signal-to-noise ratio (SNR), and crosstalk by exciting the CODECs with single and multitone signals from an Audio Precision tester. In a THD+noise test, he typically uses a 1-kHz sine wave with an amplitude 1 dB below the device's maximum input level, and he measures second and third-order harmonics with the audio tester.

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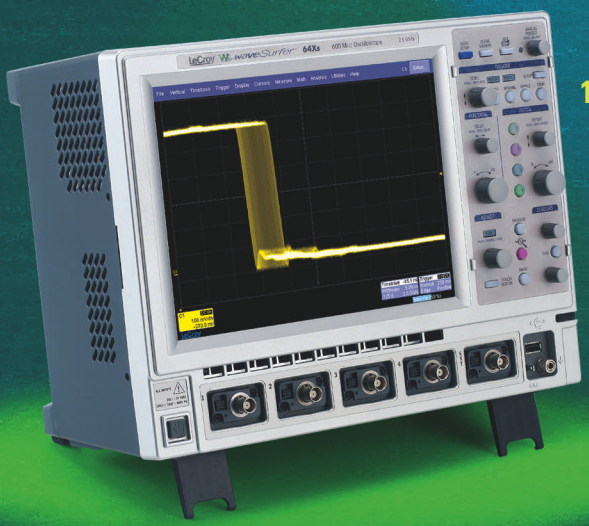

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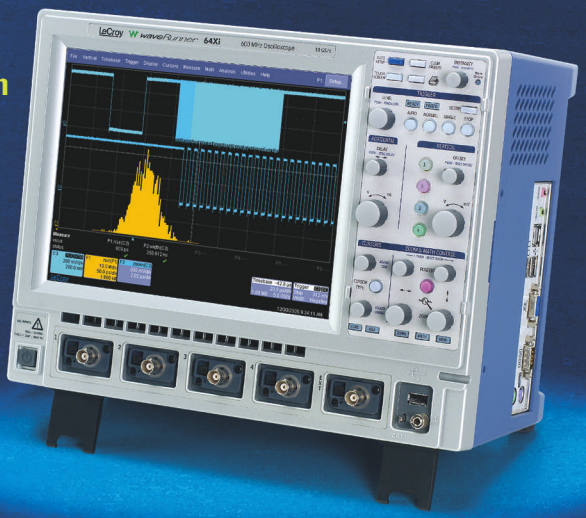

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Patel initially receives about 50 devices for evaluation and debug. As part of his bench evaluation, Patel checks for device functionality in all possible modes of operation. After the bench tests, Patel uses an ATE system to further characterize the device, looking for critical digital-interface timing limits.

Digital timing characterization may involve skewing digital signals with respect to each other, which is how Patel measures setup-and-hold time. He characterizes CODECs over the specified temperature range, power-supply voltages, and variations in the wafer-fabrication process. If the parts meet specifications, he evaluates about 500 parts on an ATE system for statistical evaluations. From the statistics, he can assign typical and guaranteed values for the part's published data sheet. The statistical measurements include the analog characteristics THD+noise and SNR.

"We typically hold back about 50% of a preproduction run of partially processed wafers in case we need to make changes," said Patel. "If changes are simply to the logic circuits of the CODEC, then new prototype parts can be ready in about three weeks. If changes are required to the device's analog circuits, a change may take as long as 12 weeks."

RF devices

Analog Devices also manufactures RF and optical components developed and tested by engineers in the RF and wireless (RFW) group. Senior product engineer Tom Kelly evaluates RF products such as power detectors, amplifiers, multipliers, and modulators as well as optical components such as log detectors. The RFW group has several automated test benches, one of which Kelly used to test the AD8349, a 700-MHz to 2.7-GHz quadrature modulator used in GSM and CDMA cell phones.

During his evaluation of the AD8349, Kelly measured noise, adjacent channel leakage ratio (ACLR), and sidebands with the test setup shown in **Figure 3.** The Aeroflex signal generator produces a carrier as well as the I and Q modulation signals. To measure the modulator's performance, Kelly measures the modulator's output spectrum with a Rohde & Schwarz spectrum analyzer.

Figure 4 shows an ACLR measurement of a two-carrier 101 W-CDMA signal. To make the measurement, Kelly modulates two W-CDMA channels spaced in frequency so that one channel separates them. Then, he looks at the signal leakage in the unused channel and at frequencies above and below the two carriers. In this case, the difference between the radio-link modulator (AD_RLM) and its predecessor, the AD8349, is about 4 dB in the adjacent channels. **Figure 5** shows the sideband measurement.

Calibration is important in measuring sideband suppression. "Traditionally, we've calibrated the signals using an HP vector voltmeter," he explained. "Since this piece of equipment is no longer supported, we're looking at using either a VNA or high-speed scope."

Kelly is concerned about how calibration affects a modulator's I and Q baseband inputs. If the signals aren't equal in amplitude and in quadrature, Kelly will see an undesired sideband. Just 1° of phase error, even with perfect amplitude match, causes a –40-dBc undesired sideband. A 1° phase and 0.5-dB amplitude error generates a –30-dBc undesired sideband.

Engineers at Analog Devices spend weeks evaluating new IC designs on the bench, on automated test stations in the lab, and on production ATE systems. A product engineer must approve a product for production, and he or she provides valuable feedback to designers. T&MW

Reader feedback

Do you work with amplifiers, data converters, CODECs, or RF modulators, either for sale to your customers or to incorporate into your products? How do your tests differ from those of the engineers at Analog Devices?

Contact senior technical editor Martin Rowe with your applications, mrowe@tmworld.com.

FOR MORE INFORMATION

The May 2005 issue of *Test & Measurement World* included an interview Martin Rowe conducted with a product engineer at Analog Devices' design center in Beaverton, OR. See "Northwest passage," www.reed-electronics.com/tmworld/article/CA528092.

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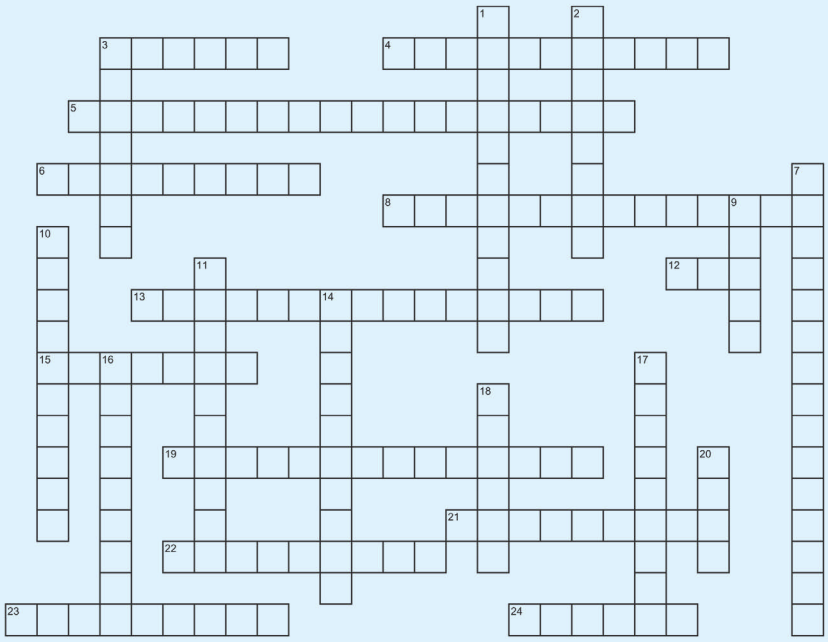

DOWN

1 System with both analog and digital waveforms
2 Sine, square, triangle, and sawtooth are examples
3 External stimulus that initiates instrument functions
7 Technique used to ensure instrument clocking occurs at the same time
9 Unwanted signals
10 The smallest amount of input signal change that an instrument or sensor can detect.
11 Next generation, high-bandwidth, high speed PC bus based on PCI
14 Frequency at which the ADC converts analog to digital data
16 -3dB below the passband frequency
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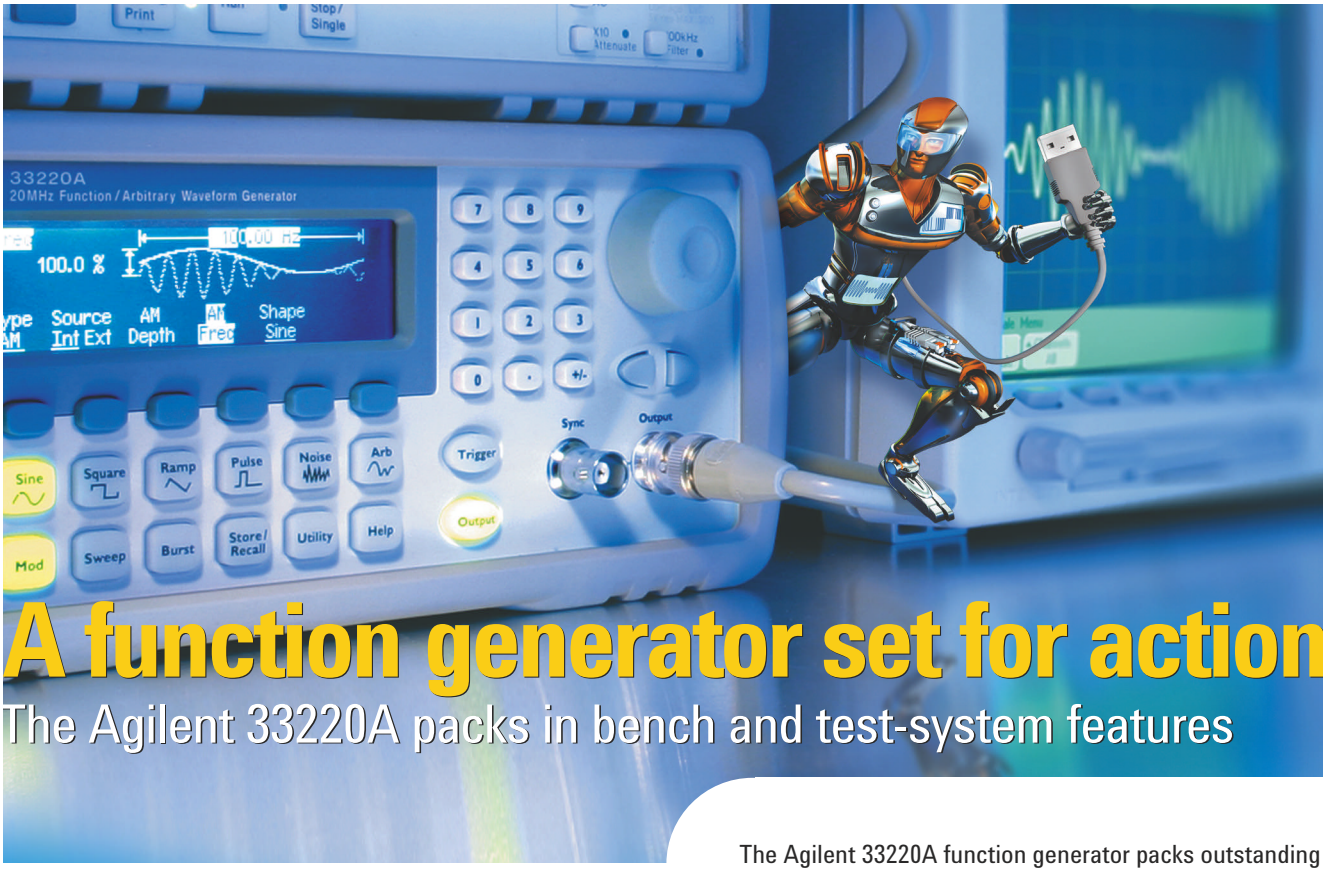

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LIMITS of TEST TIME REDUCTION

Calculating the optimal compression level will provide the highest return on silicon resources.

CHRIS ALLSUP, SYNOPSYS

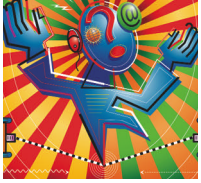
Nanometer fabrication processes offer higher circuit density and better performance but also present new challenges. Systematic and random defects that were a nuisance above 90 nm are now killer defects. To maintain quality, more test patterns must target larger numbers and more types of defects. And as circuit density increases, the number of internal scan elements, and hence the length of scan chains, increases. More scan patterns and longer scan chains can inflate test-execution time by a factor approaching the square of the die area, and SOC test costs increase by the same factor.

On-chip scan compression technology has emerged as a way to reduce test-execution costs by reducing the time spent testing digital circuits (Ref. 1). Various scan-compression architectures are available, all of which reduce test time by creating x times more scan chains with approximately x times fewer scan elements in each scan chain. Compression effectively reduces the time it takes to scan each test pattern. For a scan-compression factor of x (assuming the scan chains are well balanced with no pattern inflation issues), test application time reduction is:

$$TATR = 100(1 - 1/x) \qquad (1)$$

Note that TATR is an asymptotic function. For example, a 20-times scan compression ($x = 20$) reduces test application time by 95% (TATR = 95%), whereas a 50-times compression achieves 98% TATR. 100-times compression reduces test application time by 99%, an improvement of only 1% compared with 50-times compression.

By using a cost model, you can determine whether there are benefits in tar-



geting more than about 20-times scan compression. Some researchers (Ref. 2) have expanded upon a DFT cost model (Ref. 3) to compare different scan-compression methods, but you need an additional model to determine the optimal amount of compression.

I have developed a framework for evaluating the full economic impact of implementing scan compression. Using this model, you can determine whether additional compression offers any benefits and, if so, what the actual cost savings are. Moreover, I have developed equations that let you compare compression implementations in terms of their impact on silicon area so you can evaluate which approach is the most cost effective.

Test execution and silicon area

Companies most likely to value large reductions in test application time are those with very high manufacturing volumes where even a penny saved per die could add up to millions of dollars over the lifetime of a product. Under these conditions, very high TATR is desirable despite the fact that, as is evident from equation 1, the cost savings in percentage terms diminishes beyond 20-times compression.

The decision to add more compression, assuming it is easy to implement, comes down to a tradeoff between two costs: test-execution cost, C_{exec}, and silicon area overhead cost, $C_{silicon}$. Increasing the amount of compression to reduce test application time will continue to provide cost savings as long as the sum of test-execution cost and silicon area overhead cost continues to decline. You should therefore increase compression from a nominal level x to an optimal level λ that minimizes total cost, where $C_{total} = C_{exec} + C_{silicon}$ (**Figure 1**).

If you assume that tester utilization is high (greater than 90%) so that test-execution time for digital circuit testing is a bottleneck, and that non-tester hardware costs for test are much less than tester hardware costs, then test-execution cost as a function of compression level x is:

$$C_{exec} = \frac{R_{act} T_{test}}{Y(x)} \quad (2)$$

where $T_{test} = T_{setup} + \frac{K_{t_time}\alpha(x)A(x)^2}{x}$

and the silicon area overhead cost per die is:

$$C_{silicon} = C_s\left(\frac{A(x)}{Y(x)} - \frac{A_0}{Y_0}\right) \quad (3)$$

From equations 2 and 3, the total cost is:

$$C_{total} = C_{exec} + C_{silicon} \quad (4)$$

$$= \frac{R_{act}}{Y(x)}\left(T_{setup} + \frac{K_{t_time}\alpha(x)A(x)^2}{x}\right) + C_s\left(\frac{A(x)}{Y(x)} - \frac{A_0}{Y_0}\right)$$

In these equations, R_{act} is the cost of active testers ($/s); T_{test} is the test-execution time (s); T_{setup} is the setup time for an IC on the tester; K_{t_time} is a constant relating test time to die area (s/cm^2); and $\alpha(x)$ is a scalar that takes into consideration the fact that failing die require less test time:

$$\alpha(x) = Y(x) + \beta_{fail}[1 - Y(x)] \quad (5)$$

where β_{fail} is the percentage of good-die test time required on average to test a defective die. $A(x)$ is die area at compression level x. The amount of compression circuitry increases as the number of scan chains is increased, so $A(x)$ can be represented as a linear function of compression:

$$A(x) = A_0(1 + \gamma x) \quad (6)$$

where A_0 is the area of the die without any compression, and γ is a scan compression area scaling factor representing the fractional area increase in die size per unit increase in compression. C_s is a silicon area cost multiplier ($/cm^2). $Y(x)$ is the yield at compression level x and depends on the defect density D (defects/cm^2):

$$Y(x) = \frac{1}{1 + A(x)D}, \; Y_0 = \frac{1}{1 + A_0 D} \quad (7)$$

Cost saving at optimal level

The cost saving gained by increasing compression from x to the optimal level λ corresponding to where the total cost C_{total} reaches its minimum is:

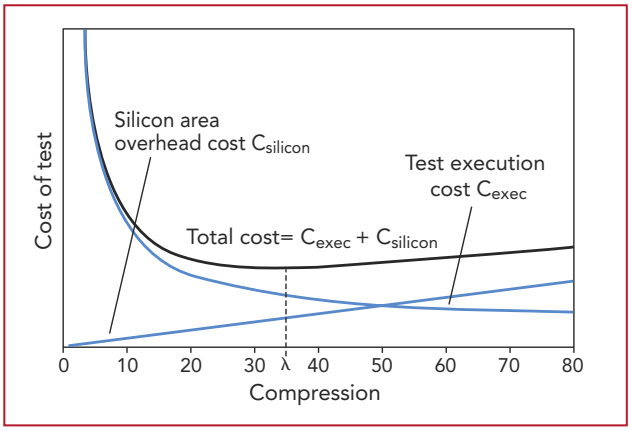


FIGURE 1. Cost of test calculations must take into account silicon area overhead costs and test-execution costs. Minimum total cost of test here occurs at λ.

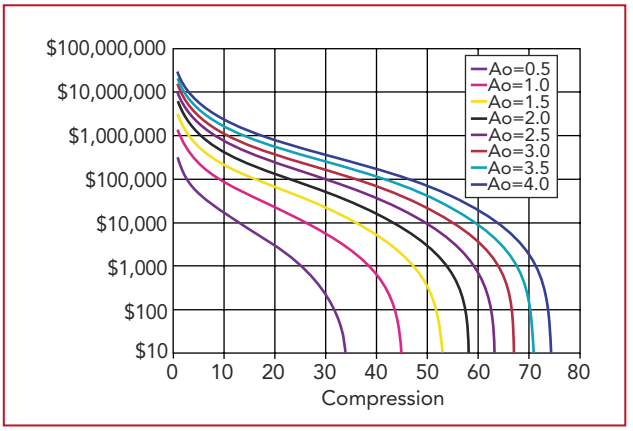


FIGURE 2. Cost savings are shown per 1 million units for different die areas, A_0. Here, D=0.3 cm^{-2}, K_{t_time}=20 s/cm^2, R_{act}=$0.06/s, C_s=$4.00/cm^2, β_{fail}=50%, and γ=10^{-4}.

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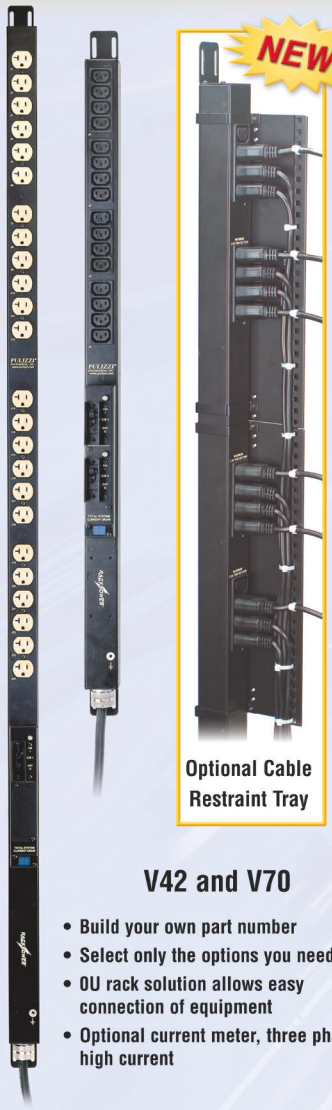

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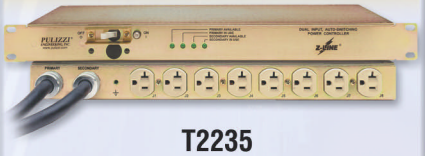

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$$\text{Cost saving} = C_{total}(x) - C_{total}(\lambda) \quad (8)$$

Figure 2 illustrates cost savings for various die areas A_0 after substituting equations 5–7 into equation 4 and then applying equation 8. The input parameters used for this example are typical of current manufacturing environments. For each compression level x, the cost saving for a particular curve corresponds to savings that would be incurred by increasing the level of compression from x to λ. (In Figure 2, values of λ are very close to the compression numbers corresponding to the lowest portion of the curves, intersecting the $10 cost saving grid line.) For example, for the curve A_0=1.0 cm^2, the cost saving gained by increasing compression from x=10 to λ=46 is just under $100,000 per 1 million units.

All designs benefit from compression, but because test-execution time is proportional to the square of the die size, the largest designs benefit the most in dollar savings. At any compression level less than the optimal compression level, there is more time left over to "squeeze" incremental savings by applying further compression.

Cost difference of compression schemes

You can evaluate the difference in test costs between two scan compression implementations, SC_1 and SC_2, assuming the same design effort but different silicon area overheads for the same level of compression. All other factors being equal, the solution with the lowest area overhead across compression levels will be the most cost effective. Using equation 6, the areas are:

$$A_1 = A_0(1+\gamma_1 x),\ A_2 = A_0(1+\gamma_2 x) \quad (9)$$

where the ratio γ_2/γ_1 represents the comparative area overhead between SC_1 and SC_2.

Consider the case in which SC_2 has a higher scan compression area scaling factor than SC_1: $\gamma_2 > \gamma_1$. The higher area scaling factor γ_2 means the optimal compression level for SC_2 (λ_2) is less than that for SC_1 (λ_1). Comparing the total cost difference between the two implementations at compression levels $x < \lambda_2$ underestimates the cost difference that is attainable when both are implemented at their optimal levels. Conversely, cost comparisons at $x > \lambda_1$ overestimate the difference. The total cost difference, Δ_{cost}, should instead reflect the difference between the two cost minima:

$$\Delta_{cost} = C_{total}(\lambda_2) - C_{total}(\lambda_1) \quad (10)$$

Substituting the relations in equation 9 into equation 4 and then using equation 10 for the cost comparisons, observe from **Figure 3** that total cost difference due to an increase in the comparative area overhead γ_2/γ_1 increases rapidly in proportion to die size.

Derived formulas for optimal compression

You can derive simple formulas to evaluate the cost savings from compression, the optimal compression level λ for a design, and the cost difference between scan compression implementations.

Nonlinear effects

Keep in mind that these results are based on the linear equation 6, which is accurate as long as the number of added gates per scan chain remains constant with increasing compression. Some compression schemes, however, may entail silicon overhead that increases disproportionately with higher compression levels. Similarly, some compression schemes entail an initial fixed amount of circuitry even for very small compression levels. To learn how to account for these nonlinear effects, see "Nonlinear effects" in the online version of this article at www.tmworld.com/2006_06.

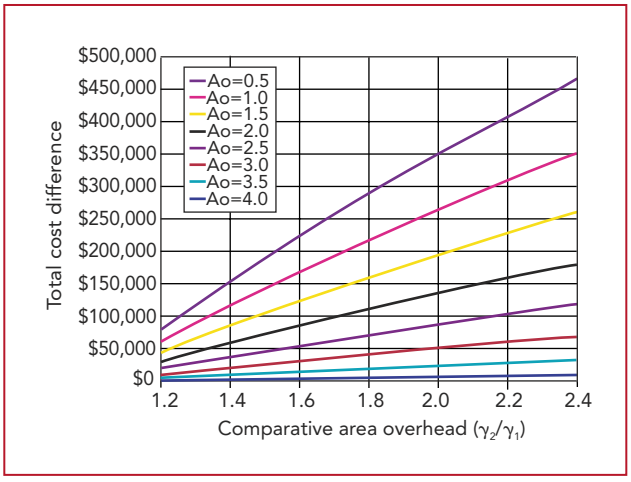

FIGURE 3. Cost difference per 1 million units are shown here as a function of γ_2/γ_1 for different die areas A_0. Here, D=0.3 cm^{-2}, K_{t_time}=20 s/cm^2, R_{act}=$0.06/s, C_s=$4.00/cm^2, β_{fail}=50%, and $\gamma=10^{-4}$.

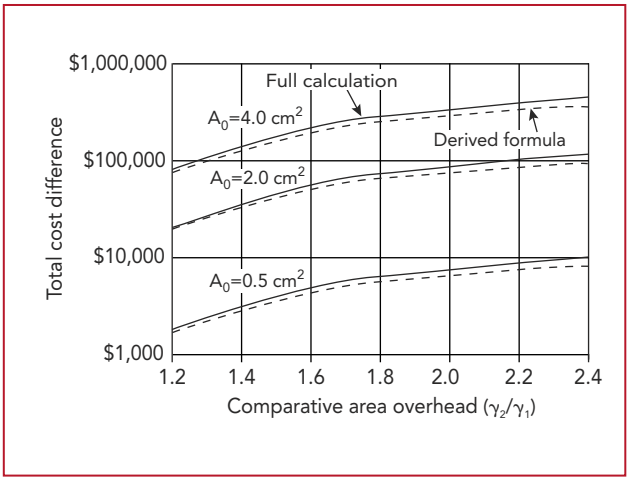

FIGURE 4. Cost difference per 1 million units as a function of γ_2/γ_1 for different die areas A_0 illustrate the accuracy of derived formulas vs. full calculation. Here, D=0.3 cm^{-2}, K_{t_time}=20 s/cm^2, R_{act}=$0.06/s, C_s=$4.00/cm^2, β_{fail}=50%, and $\gamma=10^{-4}$.

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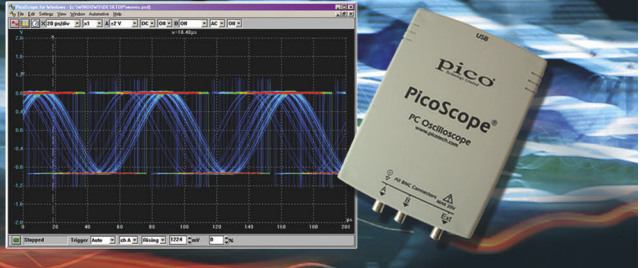

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First, T_{setup} does not influence compression tradeoff and can be ignored for comparative analysis. Second, the scan compression area scaling factor γ is small (on the order of 10^{-4}), so if you expand the expression for $A(x)$ in the equation that defines T_{test} for equation 2, you find the contribution of compression logic to test-execution time is negligible. This is reasonable from the perspective that the compression logic can be tested very quickly compared to the rest of the chip.

As a result, the expression for $A(x)$ in equation 2 can be approximated by A_0 without much loss in accuracy. Furthermore, you may simply replace the product term $K_{t_time}A_0^2$ with T_0, the test-execution time in seconds that would be in effect for a design without the use of scan compression. Assuming the scan chains are well balanced:

$$T_0 \cong \left(\frac{\#\ scan\ \ flops}{\#\ scan\ \ chains}\right)\left(\frac{\#\ scan\ \ ATPG\ \ patterns}{tester\ \ clock\ \ frequency}\right) \quad (11)$$

In addition, $Y(x)$ in equation 2 can be approximated by Y_0 because the increase in test execution cost due to the very small decrease in yield caused by adding compression circuits is negligible compared to the cost saving. Finally, note that the scalar that accounts for less time spent testing failing die has very little dependence on the amount of compression, so $\alpha(x)$ can be approximated by α_0. With these simplifications in mind, equation 4 reduces to:

$$C_{total} \cong \frac{T_0 R_{act}\alpha_0}{xY_0} + C_s\left(\frac{A(x)}{Y(x)} - \frac{A_0}{Y_0}\right) \quad (12)$$

where $\alpha_0 = Y_0 + \beta_{fail}(1 - Y_0)$.

The cost saving gained by implementing compression level x is the difference between test-execution cost without compression and total cost with compression:

$$\begin{aligned} \text{Cost saving}(x) &= C_{exec}(1) - C_{total}(x) \\ &\cong \frac{T_0 R_{act}\alpha_0}{Y_0}\left(1 - \frac{1}{x}\right) - C_s\left(\frac{A(x)}{Y(x)} - \frac{A_0}{Y_0}\right) \end{aligned} \quad (13)$$

Substituting the linear expressions for compression area (equation 6) and yield (equation 7) into equation 13 gives:

$$\text{Cost saving}(x) \cong T_0 R_{act}\alpha_0(1 + A_0 D)(1 - 1/x) - A_0 C_s \gamma x(1 + 2A_0 D) \quad (14)$$

The total cost reaches a minimum where the derivative of equation 14 is zero:

$$\frac{d}{dx}(C_{total}) = 0 \quad (15)$$

Substituting equations 6 and 7 into equation 12 and solving equation 15 for x yields this formula for the optimal compression level λ:

$$\lambda \cong \sqrt{\frac{T_0 R_{act}\alpha_0(1 + A_0 D)}{A_0 C_s \gamma(1 + 2A_0 D)}} = \sqrt{\frac{T_0 R_{act}\alpha_0}{A_0 C_s \gamma(2 - Y_0)}} \quad (16)$$

The derived formula values are accurate to within ±1.2%, standard deviation = 0.6%, compared with the entire data set of λ measured from equation 4.

You can also derive a closed expression for the cost difference between compression solutions that can be used to evaluate the cost effectiveness of alternative compression implementations. The comparison can be made by substituting the simplified form of C_{total} (from equation 12) into equation 10 and then using the derived formula of λ in equation 16 to find the cost difference. Δ_{cost} reduces to:

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$$\Delta_{cost} \cong T_0 R_{act} \alpha_0 (1 + A_0 D)\left(\frac{1}{\lambda_2} - \frac{1}{\lambda_1}\right) + A_0 C_s \gamma (1 + 2A_0 D)(\lambda_1 - \lambda_2) \quad (17)$$

Figure 4 displays total cost difference Δ_{cost} just as in Figure 3, except it focuses on three initial die areas to compare the derived estimates for Δ_{cost} in equation 17 with those obtained using the full calculation.

Scan compression greatly reduces test-execution costs, but the silicon area overhead cost of compression limits how much test application time reduction is cost effective. For any design, there is an optimal compression level proportional to the square root of the die size that provides the highest return on silicon resources. This optimal level is sensitive to the area overhead of compression and other architectural aspects. T&MW

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Chris Allsup, *marketing manager of test automation products at Synopsys, has more than 20 years combined experience in IC design, field applications, sales, and marketing. He earned a BSEE degree from U.C. San Diego and an MBA degree from Santa Clara University.*

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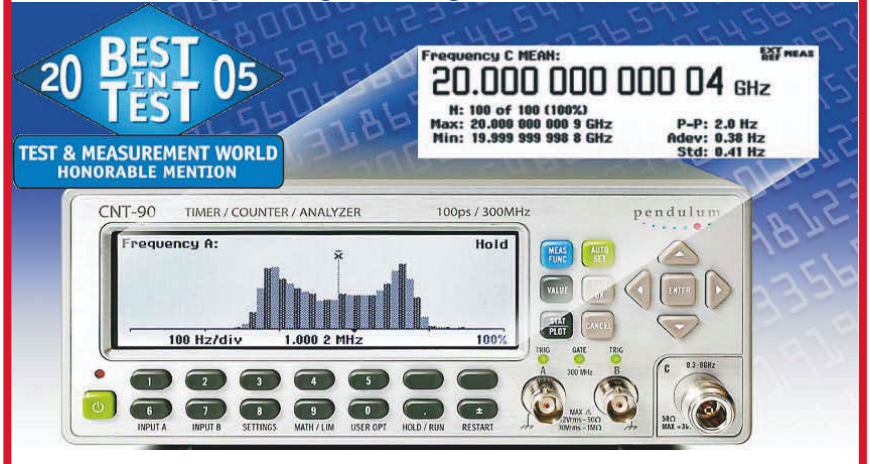

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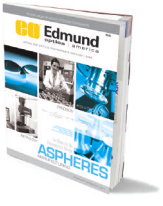

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Post-Test Inspection BOOSTS DIE YIELDS

JON TITUS, CONTRIBUTING TECHNICAL EDITOR

Wafers produced for products as diverse as LEDs and MP3 players vary greatly in function, but they have one thing in common: They often undergo optical inspection *after* they pass an electrical test.

Increasingly, wafer fabs are turning to automated optical inspection (AOI) equipment to locate defects so they can deliver known-good die and simultaneously increase their yields. Unlike human inspectors, AOI equipment consistently locates and classifies defects, and it provides information that process engineers can use to track and head off potential problems.

But why would wafers of flash-memories, LEDs, or other devices require a final visual examination? After all, they just went through an electrical test that identified faulty devices. The answer is that an electrical tester cannot identify defects such as scratches, nicks, and missing passivation material that might lead to problems later in a product's life.

Another reason is that the electrical tester itself can be the source of problems, because the movement of test probes as they touch a wafer can create defects. Individual probes should touch only a bonding pad and leave only a small mark (**Figure 1**). Smaller semiconductor geometries, however, decrease the area of bonding pads, which makes them more difficult targets for a prober to "hit."

During electrical testing, slight misalignments may cause probes to damage passivation material that surrounds a pad and thus open semiconductor areas to destructive moisture (**Figure 2**). If a probe hits a pad at too great an angle, it might scrape off metal that can cause a short circuit in a packaged device.

Even when a probe touches down in the center of a pad, the physical contact can gouge or scrape the pad, which leads to a poor bond between the pad and a connecting wire. Although enough of a wire-to-pad bond can exist to let a packaged device pass final electrical tests, later on a small stress may cause the wire bond to fail.

"In a stacked-die package, those bond pads attach to other devices," said Mike Plisinski, VP and GM of the data-analysis and review business unit at Rudolph Technologies. "So, if you have combined five expensive die and one of them has a bond-pad defect you didn't find, you have 'killed' the four good devices and wasted an expensive package."

To guard against such defects, probe-mark inspection (PMI) has become a key

IC manufacturers rely on optical inspections at the end of fab lines to catch physical imperfections as well as defects caused by final-test probers.

back-end step on wafer-fab lines. Most back-end wafer-inspection systems determine if a probe mark is too big or if a probe has run off a pad or has broken through the passivation material. Inspection results let process engineers find physical defects that could have harmed a die, even though the die passed electrical tests. The AOI equipment that examines probe marks also detects and measures the dimensions of foreign materials, scratches, polyimide delamination, photo-resist residue, and nicks on wafer edges (**Figure 3**).

In addition to detecting probe-mark defects, inspection equipment can measure the distance between a probe mark and a pad's edge. "You reject a die if a probe touched the passivation window," said Amir Gilead, VP of the semiconductor-inspection products division at Camtek, "but on some wafers, you reject a die if probe marks get too close to the passivation material. You don't want to take a chance that greater probe excursions will hit the passivation material." Process engineers preset the probe-to-passivation thresholds based on the wafer types they will inspect.

To properly inspect a wafer, inspection equipment must "learn" what a good die looks like and how to find the bond pads. That process varies from vendor to vendor.

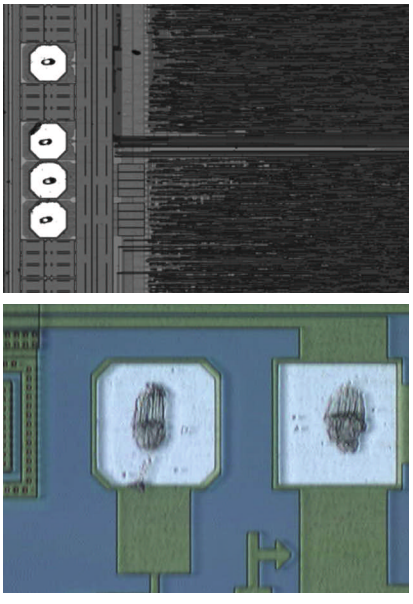

FIGURE 1. (Top) These octagonal bond pads show the small marks made by test probes. (Bottom) A close-up view shows scrape marks and the relative size of probe marks on small pads. Courtesy of Rudolph Technologies.

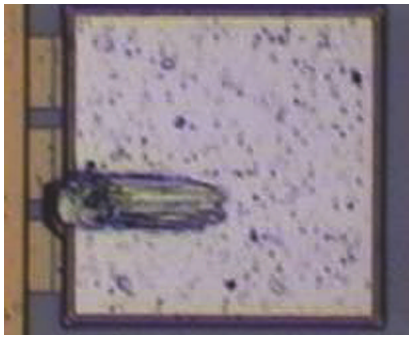

FIGURE 2. This image shows a probe mark that exceeded the limits of a bond pad and damaged surrounding passivation material. Courtesy of Camtek.

Although CAD files might simplify the training of an AOI system to locate die features, process engineers often don't have that type of information, according to Rudolph Technologies' Plisinski. "Even if they had those files, they still would have to manually align the wafer with the inspection system because lithography patterns may have shifted slightly on a wafer's surface during fabrication. So, engineers start with a wafer on a chuck in Rudolph's NSX August inspection system and go through a series of automated setup steps that take only a few minutes and depend on the required 'recipe' options."

The engineers then program the system with bond-pad characteristics. As it runs a geometrical pattern match during a wafer scan, the system automatically finds the pads. "The pad-location process takes only a few minutes," said Plisinski. "Some engineers label each pad so they can easily track changes in probe-mark characteristics or positions."

ICOS Vision Systems uses a recipe for each wafer type to set up its WI-2000 inspection station. Gert Sablon, product manager for wafer inspection products at ICOS, explained that process engineers start with an example wafer on which they locate a perfect or close-to-perfect die. An image of that die provides the reference for comparisons and becomes part of the recipe. The recipe also contains reference information about other types of defects, such as nicks, scratches, and so on. Software compares scanned wafer images with the reference image and groups visual features into defect categories that process engineers have established.

Carl Smets, research and development director at ICOS, stressed the importance of proper alignment in an inspection system. "If you have diced wafers or diced wafers on hoop rings, slight stretching may change the position and orientation of the die from what you would find on an undiced wafer. So, to inspect the wafer properly, you must perform an accurate alignment for individual die." (See "What's a hoop ring?" p. 49.) ICOS employs scalable DSP processors in its inspection system to align die positions with recipe information that includes a reference-die image.

The Falcon 500 from Camtek requires about 15 min to set up. Instead of relying on a known-good die, the system uses a proprietary technique that scans die on a production wafer to create a "clean-reference" image for comparison.

"A user or process engineer doesn't have to know in advance which wafers or die are good," explained Camtek's Gilead. "They can even take bad die with defects and still generate a good reference. A minimum of five die will provide a clean-reference image, although engineers report using an average of seven to nine die. They can increase the number of die scanned when they observe wide color variations across a wafer." Process engineers can schedule "relearn," or update, scans that let the system adjust to process variations. (Camtek has several patents pending on its inspection technologies.)

After the learning step, operators can set run-time parameters such as the sizes of defects and the acceptable sizes of probe marks. "Some engineers may want to find defects above 25 microns," said Gilead. "So, they set the system to ignore anything 25 microns or smaller. They have complete control of inspection criteria."

Classify defects

After an inspection system acquires die images, automatic defect-classification software sorts defects into categories such as scratch, pit, or probe mark. The recipe for a given wafer type includes defect classifications and parameters.

"The classifications depend on what users require," explained Smets of ICOS. "You can classify a scratch as a long object with a length greater than x and a width greater than y. But pits, for example, are typically round, so they have only a diameter dimension. Process engineers combine characteristics such as position,

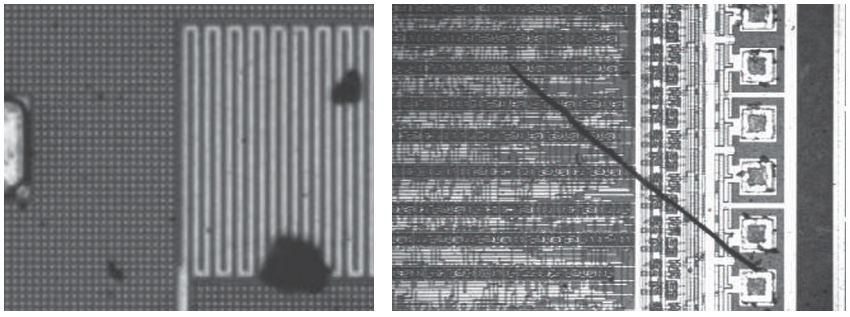

FIGURE 3. Post-test inspection software can detect and classify defects such as (left) foreign materials and (right) a scratch. Courtesy of ICOS Vision Systems.

dimensions, and optical contrast with logical operations such as AND, OR, and IF to classify defects."

The economic benefits of post-test inspection center on how many die a system can inspect in a given time and how many "false calls" its software produces. (A false call identifies a defect where none exists.)

"Engineers see a wafer move quickly on a chuck and think speed is everything," said Gilead of Camtek. A company's profits depend to a great extent on how many wafers it can inspect in a day, not just to how fast it can scan each wafer, so productivity calculations must include setup times as well as scanning speeds. "Say it takes two hours to set up System A and 15 minutes to set up System B," said Gilead. "If you inspect three types of wafers in a day, you spend six hours versus 45 minutes on setup. Even if System A scans faster than System B, the latter may offer a higher efficiency."

Engineers also should pay attention to the balance between scanning speed and the size of the defects they want to detect. Equipment may offer a scanning speed of *x* wafers/hr and a capability to detect defects as small as, say, 2 μm. But an inspection system cannot provide both capabilities simultaneously, cautioned Gilead. "If you need a higher resolution, or a higher magnification, to find smaller and smaller defects, the inspection speed decreases in proportion."

At the end of an inspection run, software identifies defective die so process engineers or operators can "reverify" the defects found. People review the defects and classify them as critical or noncritical. This process requires extra time and money, and cuts productivity, but you may need to do it.

Suppose your AOI system reports 20 defective die, but unknown to you, only three have critical defects. Can you afford to throw away all 20? Probably not. So you inspect all 20 and scrap only the three bad ones. The reverification step not only reclaims good die, but also lets you tighten your inspection criteria so subsequent inspections identify fewer false-call defects. But you must balance the benefits of eliminating false calls against the possibility that tighter specs will let AOI software pass defective die.

Economic benefits accrue from another aspect of post-test inspection—

What's a hoop ring?

You cannot cut a wafer into individual die (also known as singulated die) without some sort of supporting material that holds die in place during and after slicing. That flexible material, called wafer mounting tape, sticks temporarily to the back of a wafer. Additional processing steps may require that die remain in place for testing, inspection, or packaging operations.

To make the flexible tape more rigid, you position the die-tape combination over a small "hoop" and press a larger concentric hoop over the smaller one. The process stretches the tape slightly and forms what looks like a drum head. (Embroiderers use a similar set of hoops to stretch material so they can stitch patterns through semi-rigid cloth.) Exposure to ultraviolet light reduces the tape's adhesive capability and releases individual die for packaging.—*Jon Titus*

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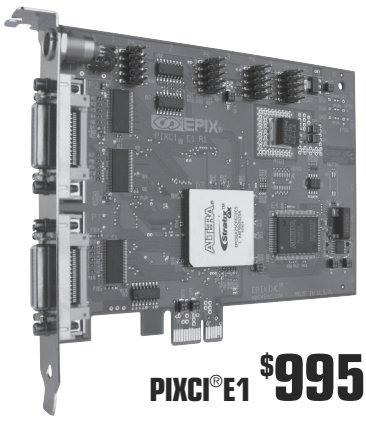

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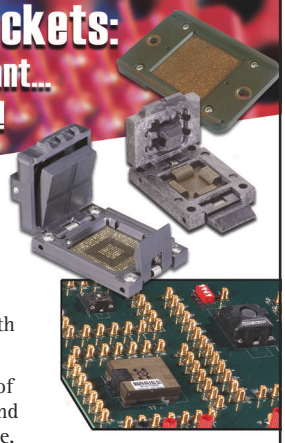

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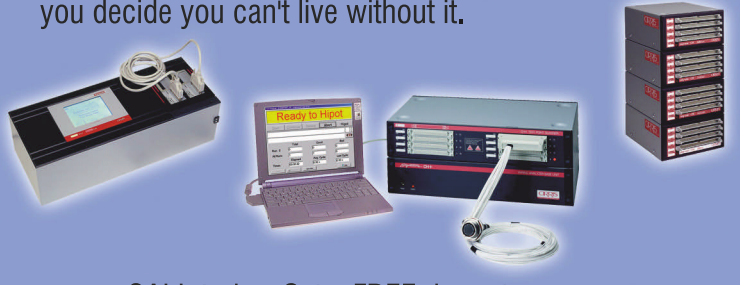

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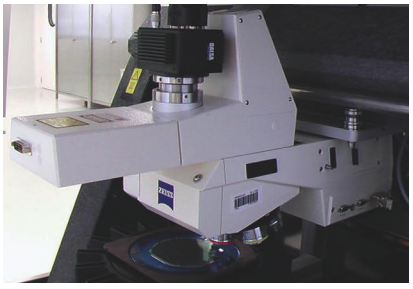

This image shows the arrangement of a microscope and camera in the WI-2000 wafer-inspection equipment. The wafer moves underneath this assembly.
Courtesy of ICOS.

statistical process-control (SPC) information derived from inspection results. Using this quantitative information, equipment operators can identify and correct immediate problems. In addition, process engineers can examine long-term trends to determine, for example, why a probe pin has gone out of alignment or shows an excursion toward the edge of a bond pad.

"Say probe marks start to drift to the left and cause defects," said Plisinski of Rudolph Technologies. "The engineers see this trend, determine which prober causes the problem, and correct it. Or they may use the SPC data to uncover a problem with their alignment recipe."

The inspection information also lets engineers "stack" images to look for wafer-to-wafer trends. If they see scratches in the same place on many wafers, the SPC information can lead them to a robot end effector as the problem, explained Plisinski.

Until now, you may have thought a final electrical test provided the last word about the quality of your die. Placing an inspection system after the last test station, though, will help you weed out defective die you didn't know existed, keep test processes in control, and reduce field failures. T&MW

Pre-test inspect, too

Some companies have found a benefit in performing pre-test inspections. Small dust particles on 300-mm wafers can provide enough mass to permanently reposition—and damage—tiny test probes. In effect, these "killer" particles can shut down a fab line. (The cost of a ruined probe card for large wafers may amount to more than the cost of inspection equipment.)

"The need for pre-test inspection came as a surprise," said Camtek's Gilead. "In a Class-100 or Class-1000 clean room, you wouldn't think dust particles on a wafer would cause concern. But even in a controlled environment, once in a while a killer particle will come along and cause a catastrophe. Simple inspections can prevent that from happening."

Jon Titus

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Sample Clock Rate	50S/ s to 1.2MS/ s	50kS/ s to 1GS/ s
Memory Size	8 Meg (16 Meg optional)	4 Meg
Memory Management (Sequences/ Steps)	1 / 4,096	1 / 8,000
Vertical Resolution	12 bits	10 bits
Modulation	FM, FSK, PSK, sweep and more	N/A
Max Frequency (Sine/Square/others)	125MHz/ 125MHz/ 125MHz	100MHz/ 100MHz/ 100MHz
Max Amplitude	2Vp- p	2Vp- p
Connectivity	LAN, USB and GPIB	LAN and GPIB
Warranty	5	1
Price Starts at	$12,495 *	$32,400

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Specification compiled from Tabor 1281 data sheet and Tektronix AWG520 data sheet 76W_11846, August 26, 2004. Prices are taken from the vendors websites. Exclude VAT.

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PXI Express set to speed PXI market

Richard A. Quinnell, Contributing Technical Editor

National Instruments is recognized as a world leader in the development of PXI software and instrumentation. Recently, I called Richard McDonell, NI's PXI marketing group manager, to ask about the future of PXI.

Q: How is the PXI market doing?
A: PXI has been the fastest growing part of our business, at or above 40% annually, and market research firm Frost & Sullivan expects it to be the fastest growing segment of the test-and-measurement market for the next five years.

Q: But the PCI bus on which PXI is based is running out of steam in the face of today's gigahertz processors. What does that imply for PXI?
A: The buzz today in the marketplace is PCI Express. It has pretty big shoes to fill if it is to replace PCI, which is still selling well and has a tremendous installed base. But PCI Express is exactly the bus that National Instruments has been looking for. The way PCI Express is architected it does a fantastic job of extending PCI. It can achieve 45 times the bandwidth of PCI and it provides dedicated bandwidth, not shared. That's up to 2 Gbps of dedicated bandwidth.

Q: What is the status of the PXI version of PCI Express?
A: The PXI Express specification was finalized in August 2005. We plan to introduce a PXI Express chassis and controller board this spring, and we know of at least half a dozen other vendors with PXI Express products in development. *(Ed. note: See box, p. 54.)* And it's important to note that PXI Express and PXI are completely hardware and software compatible so applications can move to PXI Express quickly.

Q: What other benefits besides greater bandwidth does PXI Express bring to the party?
A: Along with the increased capacity, there is better synchronization available. The bus offers a shared 100-MHz clock for synchronizing actions within the chassis. PXI had a 10-MHz clock, so this represents more precise timing.

Q: Are there applications that require the extra capabilities of PXI Express?
A: The market will be going after high-speed digital applications such as streaming video, machine vision, and semiconductor ATE. The extra capabilities of PXI Express allow creation of high-frequency, high-channel-count systems that are difficult to implement in PXI. Imagine being able to handle 60 channels of 100-MHz streaming video simultaneously or recording RF signals live to a RAID system—PXI Express can do it.

Richard McDonell, PXI marketing group manager for National Instruments.
Courtesy of National Instruments.

Q: Do you think PXI Express will spell the end of PXI?
A: It's very rare that one size fits all. We will need PXI Express for the highest bandwidth applications, but there are many things besides performance that will attract end users to PXI. These include its low cost, compact size, and design flexibility. Despite the fact that there are more than 1200 PXI products available today, more often the limitation of PXI is the lack of a particular PXI module and not performance of the PCI-based PXI backplane.

Thus, there is growing importance in PXI serving as the core of hybrid test systems and a growing opportunity for more vendors in the PXI marketplace. National Instruments, working with the PXI Systems Alliance, will continue extending PXI through research and by expanding its ability to meet new applications. □

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EDITOR'S NOTE

Innovation's one-two punch

Richard A. Quinnell, Technical Editor

Innovation never seems to come in one big burst. Instead, it is a one-two punch.

For PXI Express, the first punch was the creation of the technology itself. Creating a high-speed, serial data-handling bus that faithfully mimics the behavior of the older parallel bus required a combination of inspiration and clever execution. Those attributes essentially define innovation.

The immediate result of creating PXI Express will be a tremendous boost in the data-handling capability of PXI-based instrumentation. PXI Express offers more than 40 times the data bandwidth of PXI while offering complete software compatibility with PXI.

The second punch is now the one to look for. Whenever an innovation provides a jump in the performance of an existing capability, it usually follows that up with something entirely new. Engineers will inevitably discover that they can now implement a design that was previously not feasible. With this discovery will come inspiration, and wholly new applications and design approaches will appear. The innovation in equipment thus produces innovations in applications, the second punch.

While the first punch is essential to what follows, it is this second punch where fortunes are won or lost. The new applications and approaches will open significant revenue opportunities for those who pioneer them. Study that first punch carefully so you can determine where to land the second. □

Contact Rich Quinnell at richquinnell@att.net.

HIGHLIGHTS

Goepel looks to PXI Express

During the recent Virtual Instruments in Practice (VIP) event sponsored by National Instruments Germany, Goepel electronic introduced the development of a new series of JTAG/boundary-scan controllers with PXI Express interfaces as part of its ScanFlex boundary-scan hardware platform. The prototype of the new ScanFlex Boundary Scan controller family (SFX controllers) is named SFX/PXIe1149-(x) and includes three models for different performance classes, which differ in offering maximum TCK frequencies of 20, 50, and 80 MHz, respectively.

The new controller family's x1 configuration achieves transfer rates up to 264 Mbytes/s in zero-wait-state burst mode and is based upon the PXI Express hardware specification 1.0. In combination with additional modular ScanFlex components, PXI Express-based boundary-scan systems with up to eight Test Access Ports can be configured and synchronized with other functional modules. All TAPs provide programmable input and output voltage as well as programmable input and output impedance. Furthermore, resources such as 32 dynamic I/O, two analog I/O channels, three static I/O, and trigger lines are standard features.

"We rate PXI Express as one of the most important strategic test and measurement standards for modular instrumentations with an enormous market potential in the future," said Thomas Wenzel, director of the boundary-scan business unit at Goepel electronic. "The new series of SFX controllers will be the first to apply the PXI Express standard's performance to extended JTAG/boundary-scan applications. On this basis, an unrivaled data throughput for complex tests, as well as high-speed in-system programming of Flash and PLD components, can be achieved." www.goepel.com.

NI introduces PXI Express chassis and controllers

National Instruments has released what it calls the industry's first PXI chassis and controllers based on PCI Express signaling. The company says these PXI Express products are ideal for high-channel-count, high-throughput, or multimodule applications, such as IF streaming, mixed-signal, and image acquisition. (PXI Express integrates PCI Express signaling into the PXI standard.)

The NI PXIe-1062Q chassis offers up to 1-Gbyte/s per-slot dedicated bandwidth and eight card slots: a PXI Express system slot, a PXI Express slot with system timing capabilities, four PXI peripheral slots, and two hybrid slots that accept both PXI and PXI Express modules. The NI PXIe-8103 embedded controller includes a 2.0-GHz Intel Pentium M 760 processor and offers 250 Mbytes/s per-slot dedicated bandwidth for up to 1 Gbyte/s of total system bandwidth.

Other available controllers include the MXI-Express for PXI Express controllers, the NI PXIe-PCIe836x, and the NI PXIe-ExpressCard8360. These controllers offer desktop PC and laptop computer control of PXI Express systems with up to 250 Mbytes/s of cabled system bandwidth.

The new PXI chassis and controllers work with all existing PXI modules and software. Engineers can use existing code written for NI's LabView, LabWindows/CVI, and Measurement Studio. www.ni.com.

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PXI tackles processor benchmarks

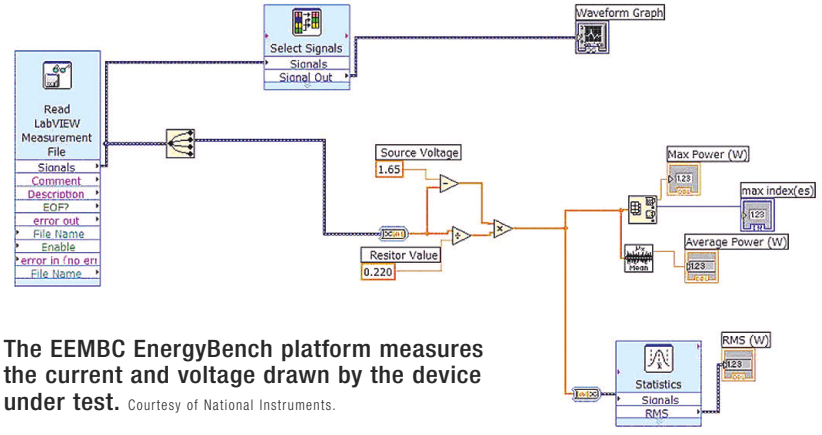
Richard A. Quinnell, Contributing Technical Editor

Predicting the performance of an embedded processor in an application is a challenging task that requires careful control and measurement. The Embedded Microprocessor Benchmark Consortium (EEMBC) has developed a series of software tests to facilitate making such predictions as well as to facilitate comparison-shopping among design alternatives (Ref. 1). Now, EEMBC is using PXI technology to tackle its latest benchmark effort: power utilization.

A key factor in most portable system designs is the power consumed during operation. This power usage affects battery size, operating lifetime between battery charges or changes, packaging design for thermal management, and weight, all trading off against device performance and features. The ability to evaluate the power performance of design alternatives is thus a significant need in the portable device market.

The EEMBC has addressed this need with the creation of its EnergyBench power and energy benchmark. EEMBC president Marcus Levy explains that EnergyBench simultaneously measures system performance and power consumption of embedded processors with all of their built-in I/O peripherals. The resulting score is a metric that product developers can use to evaluate their designs and that processor vendors can use to promote their product's efficient use of energy.

To make benchmark scores useful for industry-wide comparison, however, EEMBC has to certify the scores. "For us to certify benchmark scores," said Levy, "we need vendors to send in their test platforms. We don't want all kinds of homemade versions being sent in, so we defined a standard platform." That standard platform uses PXI instruments running LabView software to control the test and make measurements.



The EEMBC EnergyBench platform measures the current and voltage drawn by the device under test. Courtesy of National Instruments.

Control of timing is key

As shown in the **figure**, the benchmark platform monitors the power source voltage and measures the current passing to the device under test (DUT) by using a sense resistor. This requires only a modest data-acquisition capability that is not unique to PXI. The control and timing features of PXI, however, are critical to making the right measurements.

According to Levy, the platform starts and stops the running of benchmark software and keeps the execution synchronized with the power measurements. "We need to coordinate data collection with the benchmark run," said Levy. "Further, we needed to control the timing of the sampling. The scores are based on several runs of the benchmark software, and we need to alias the sampling times on the multiple runs to ensure that we are not sampling on the same processor event each time."

To fully exercise the processor and I/O, the platform also generates signals and measures response times for such parameters as I/O and interrupt latency and context switch times. The platform further controls overall test timing. Because power consumption varies with temperature, for instance, the platform exercises the processor for 30 min to warm it up before running the benchmark. The platform also automatically completes the required number of runs.

The choice of PXI as the basis for the power benchmark is due partly to its ability to provide all of the necessary timing and control functions. Cost was another issue. "EEMBC customers are always concerned with their budgets," said Levy. Finally, there was the human element. "We considered making a custom board, but that becomes a political nightmare as we address the question of which processor to use," Levy explained. "PXI was a much easier approach politically as well as technically."

The PXI standard platform for processor power benchmark testing is only the beginning of PXI's use within EEMBC. The same test setup can be used to evaluate telecom and networking devices using the appropriate EEMBC benchmark software. PXI's modularity also allows it to accommodate new benchmarks as they become defined. "We could add new hardware if needed or even just make changes at the LabView level," said Levy. Automotive benchmarks based on the PXI platform are already planned. □

REFERENCE

1. The EEMBC was originally named the EDN Embedded Microprocessor Benchmark Consortium, because it arose from a "hands-on" project conducted for *EDN* magazine in 1996. There is no relationship between *EDN* and the EEMBC.

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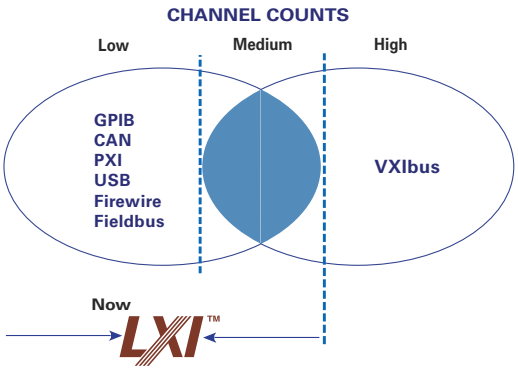

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Riding the PXI wave

Richard A. Quinnell, Contributing Technical Editor

Test instruments based on the PXI standard have been rapidly gaining ground in the test-and-measurement market, generating increased business for companies that have caught the wave. One such company, Geotest—Marvin Test Systems, has seen enough growth to require a move to larger quarters in order to meet demand. I phoned company president Loofie Gutterman, also the president of the PXI Systems Alliance (www.psia.org), to discuss the reasons behind the surging interest in PXI.

Q: So, business was booming so much that you had to expand?
A: Yes, we ran out of room. We saw a growth rate of 25% last year and are forecasting 35% to 40% this year. We needed more space for engineering, production, and integration. We were literally working in the hallways.

Q: What's causing this surge in interest in PXI?
A: There are two things happening. One is growing acceptance of PXI in markets such as mil-aero. Also, there is a rotation from other types of systems to PXI.

Q: What kind of systems are moving to PXI?
A: Modular instrumentation technology such as VXI is moving over. VXI is getting long in the tooth, suffering from obsolescence, and nothing really new is being developed. The data bandwidth for VXI just isn't there, so new programs looking for modular instrumentation are turning to PXI. It's amazing the performance being squeezed out of PXI now. Size is another factor. Users are looking for a smaller footprint.

Q: What are the new applications areas that PXI is entering?
A: There are a couple of areas that PXI is entering. One is semiconductor test systems. Companies are under pressure to get their costs down. One way to do that is to use open architecture test systems where there are multiple suppliers for the equipment, and companies are turning to that approach. The Semiconductor Test Consortium OpenStar platform, for instance, is getting PXI. This approach also has the benefit that customers can build on the platform themselves.

RF is another applications area for PXI that is growing. There has been an amazing increase in RF capabilities for a modular platform. Companies are delivering products now that operate up to 6 GHz, fast enough for cellular testing. And they keep ratcheting up performance all the time.

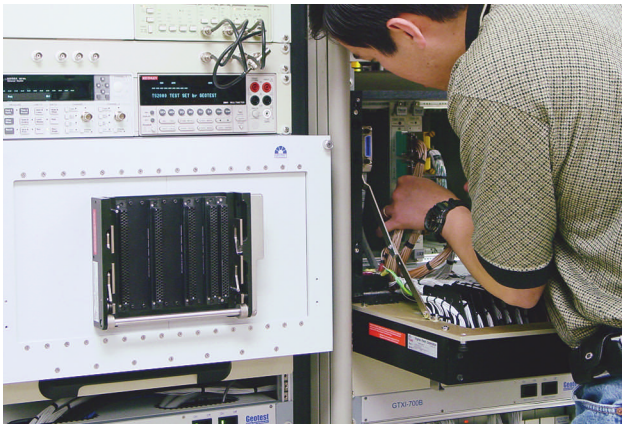
Q: What do you see as the keys to success in the PXI market—ones that give you the ability to ride the wave?
A: One is to keep on the forefront of technology. Companies need to continuously come up with new technology, performance increases, and innovative new products. You also need to spend a lot of time with customers, to keep pace with what they really want. For instance, we have found it best to offer both 3U and 6U products. Most companies only offer 3U products, but having both form factors allows us to cover more applications.

Loofie Gutterman, president of Geotest and the PXI Systems Alliance, speaks out on riding the wave of interest in PXI.
Courtesy of Geotest.

Geotest has an advantage in that we have a system-integration business in addition to manufacturing, so we are users of our own products. We get to see how usable our products are, and our internal users help refine the product. That way, our customers get a product that was not only designed for test but was successfully used in test before it got to market.

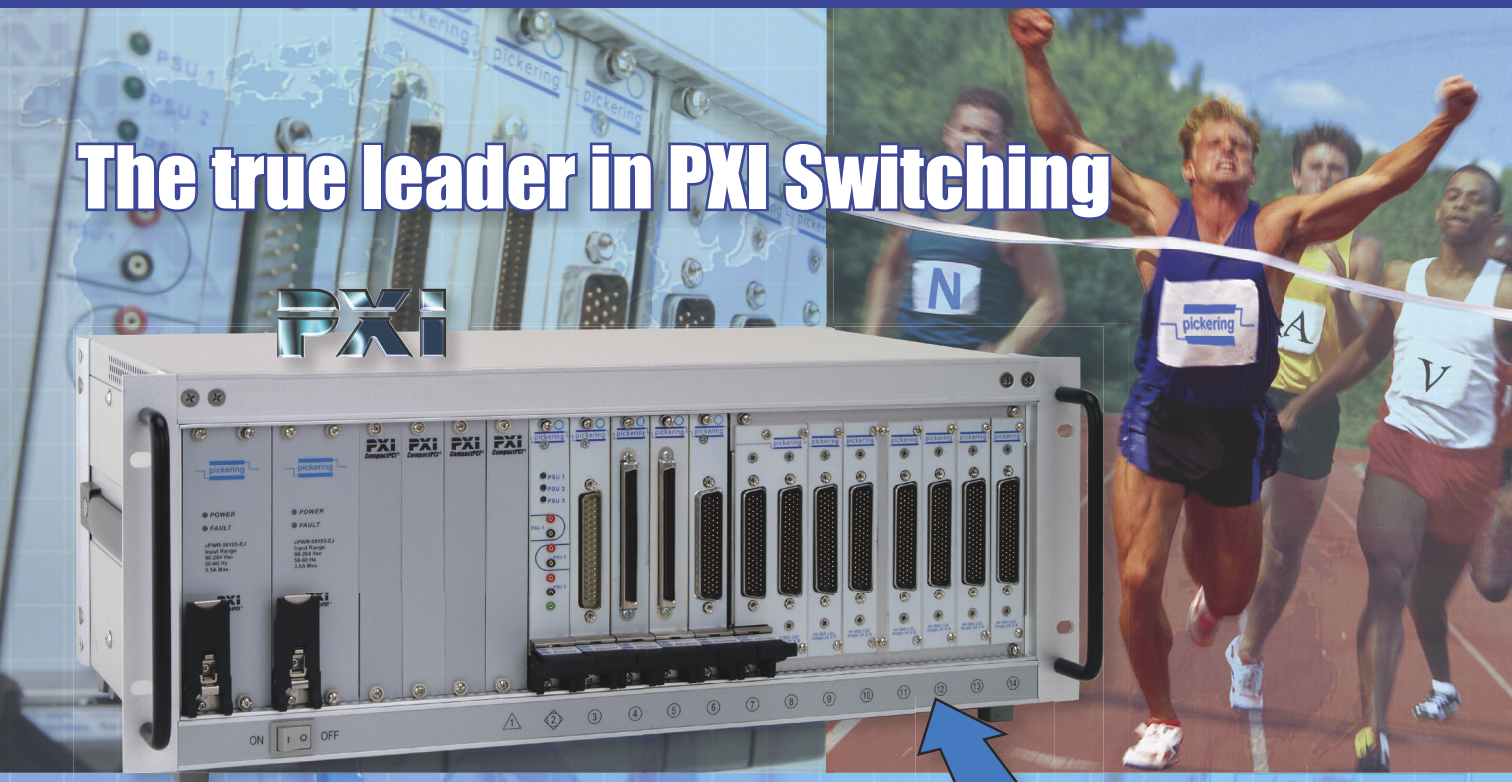
Technical support is also a key. Most PXI vendors give good instrument support; they know how their product works. Our support people are experienced test engineers, so they know how the product works and how to test. This lets us help customers use the equipment more efficiently in their application.

All these things are letting us keep pace, or better, with the growing PXI market. □



Using its own products in its system-integration business helps keep Geotest on top of the PXI wave.
Courtesy of Geotest.

PICKERING - SERIOUS ABOUT PXI



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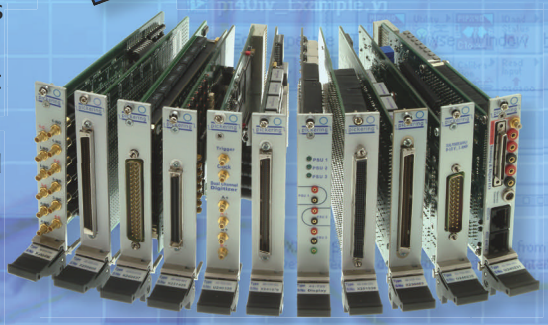

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PRODUCTS

Module simulates batteries

Pickering Interfaces has introduced the 41-750 battery-simulator PXI module that behaves as a battery supplying power to handheld and portable electronic devices in manufacturing test. The 3U single-slot module can supply up to 6 V at 2.8 A to remote loads. Typically, its transient response is <10 µs when delivering power to loads 2-m distant. You can program output voltage and set the module to source 2.8 A or sink current 0.5 A in order to test charging or discharging behavior. The module's output can float ±50 V relative to ground to fully simulate battery isolation.

A monitor port allows you to measure voltage and current with a DMM, and an inbuilt switch allows the DMM to monitor multiple simulators by daisy-chaining monitor ports. *Pickering Interfaces, www.pickeringtest.com.*

PXI chassis gains features

Geotest—Marvin Test Systems has added several new features to its GX7000 6U series of PXI chassis. The 20-slot GX7000A chassis features per-slot temperature monitoring, system power-supply monitoring, and software-controlled PXI trigger mapping. Available in desktop, rack-mount, and ITA configurations, the GX7000A accommodates up to 19 3U or 6U PXI or cPCI instruments. Slot 1 is dedicated for an embedded or remote controller, slot 2 can be used by a PXI star trigger controller or by a PXI/cPCI instrument, slots 3 through 15 provide star trigger support, and slots 16 through 20 accommodate PXI or cPCI instruments without the star trigger. The GX7000A provides an integral 10-MHz PXI clock and is available with 800 or 1100 W of system power. *Geotest—Marvin Test Systems, www.geotestinc.com.*

Test system leverages PXI flexibility

To enable expansion as production test needs change, Digitaltest is offering the MTS300 Sigma test system with PXI-based instrument options. Sigma test systems provide analog and digital in-circuit test capabilities, vectorless testing, functional test, boundary scan, and onboard programming. Designed for high throughput, the MTS300 performs up to 1000 measurements/s.

Initially, the system will be configured with a National Instruments PXI-6115—a multifunction data-acquisition card that provides two 12-bit analog outputs, eight digital I/O lines, two 24-bit counters, and analog triggering. Other boards are available on request.

An inline version of the Sigma tester is available with a PXI rack to allow for system expansion as well as rack space for VXI and IEEE 488 instruments. *Digitaltest, www.digitaltest.de.*

6-U module features 128-channel I/O

Taiwan-based Adlink Technology has introduced the 6U high-density cPCI-7452 CompactPCI or PXI module with 128 channels of digital I/O. Optical isolation protects all channel inputs and outputs up to 2.5-kV RMS. All outputs use an open-collector Darlington configuration with up to 500-mA switching capacity. The module includes a change-of-state detector that outputs an interrupt on any state change. The module supports Windows or Linux operating systems and comes with drivers for development environments such as C, Visual Basic, Delphi, LabView, or Matlab. *Adlink Technologies, www.adlinktech.com.*

Signal generators output DC to 6.6 GHz

National Instruments has announced a range of PXI 3U single-slot signal generators with outputs from DC to 6.6 GHz. The NI PXI-5650, PXI-5651, and PXI-5652 output from 500 kHz to 1.3 GHz, 3.3 GHz, and 6.6 GHz, respectively. Phase noise is typically −110 dBc/Hz at 1-GHz and 10-kHz offset. All models use direct digital synthesis generation, which readily enables analog or digital modulation for FM, FSK, or BER testing. On-off keying enables amplitude modulation. *National Instruments, www.ni.com.*

Test & MEASUREMENT WORLD

PXI Test Report is published in the February, June, and September issues of *Test & Measurement World.*

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Keithley enters pulse generator market

Keithley Instruments has introduced two pulse/pattern generators, the single-channel Model 3401 and dual-channel Model 3402. Both produce pulses at speeds up to 165 MHz with pulse widths down to 3 ns. The instruments let you adjust pulse parameters such as rise and fall times from 2.5 ns to 200 ms. You can also adjust amplitude, time delay, and offset of a pulse.

The instruments operate in four modes. Pulse mode provides one pulse per internal or external trigger.

Burst mode lets you initiate a series of pulses with a single trigger. Pattern mode lets you produce PRBS patterns in return-to-zero or non-return-to zero formats with pattern lengths from 2^5–1 to 2^{14}–1. External width mode lets you combine two or more instruments with a single external trigger.

The instruments are available with rear-mounted terminals for rack-mounted applications or with front-panel terminals for bench applications. You must specify the location at the time of ordering.

Prices: Model 3401—$12,500; Model 3402—$17,500. *Keithley Instruments. www.keithley.com.*

AOI system boasts fast setup, small footprint

With the M1 Series automated PCB inspection system, operators typically take less than 30 minutes to create a complete inspection program, its vendor reports. The M1 Series uses a standard package library to simplify training and ensure program portability across manufacturing lines.

Offering 3-Mpixel resolution and telecentric optics, the M1 Series inspects solder joints and verifies correct part assembly, all within a footprint that is less than 1 m wide. It provides the defect coverage and low false-call rate necessary to reduce costs, improve quality, and increase throughput in high-volume manufacturing environments. The system adapts to pre- or post-reflow inspection and supports rework and data-tracking requirements.

Base price: $82,500. *YESTech, www.yestechinc.com.*

ProVision assists boundary-scan development

JTAG ProVision is designed to accelerate and simplify the development of boundary-scan applications based on the IEEE 1149.x standards. The product's application wizard is aimed at engineers with minimal boundary-scan knowledge or experience. The wizard leads users through the sequence of steps to prepare test and in-system programming applications. Graphical tools simplify the management of design data for all boundary-scan applications without compromising design accessibility or test coverage.

JTAG ProVision creates a full set of tests and in-system programming functions, automatically analyzing the boundary-scan and non-boundary-scan portions of a design. JTAG ProVision can handle multiple levels of target complexity from single boards with one or more Test Access Ports (TAPs) through complex, multi-board configurations.

Base price: $11,500 for a node-locked, Windows-based license. *JTAG Technologies, www.jtag.com.*

Sapera adds geometric search

The Sapera Essential machine-vision software toolkit bundles board-level acquisition and control, image-processing capability, and a new geometric search tool. Compliant with Dalsa Coreco's Trigger-to-Image reliability framework, Sapera Essential includes image-processing libraries that provide morphology, filter, segmentation, transform, and measurement functions and that support point-to-point operations with subpixel accuracy. The geometric search tool uses edge- or area-based techniques. The software also supports blob analysis and offers 1-D and 2-D bar-code capability.

Base price: $800. *Dalsa Coreco, www.coreco.com.*

Software performs WLAN roaming tests

VeriWave's WLAN Roaming Test application measures the performance of WLAN systems as clients roam between access points (APs). The software runs on the company's WaveTest 90 and WaveTest 20 traffic

generators/analyzers to help manufacturers fine-tune the performance of wireless networks that are designed to support thousands of mobile devices.

The latest addition to VeriWave's WaveApps series of applications, WLAN Roaming Test can conduct automated, repeatable tests of roaming capabilities throughout the development, quality assurance, and deployment of large-scale WLAN systems. Metrics that can be established include roaming delay, call quality during roaming, and the network's overall ability to support large numbers of mobile clients.

Price: $6000. *VeriWave, www.veriwave.com.*

Connect to VXI over Ethernet

VXI Technology's EX2500 lets you control a VXI chassis and instruments over an Ethernet link. This slot-0 controller lets you remotely control a VXI chassis with Cat5 cable over distances up to 200 m. With a fiber-optic link, you can control a VXI chassis and its instrument modules from as much as 10 km away. Data transfer rates can reach 40 Mbps.

The EX2500 is VXIplug&play compliant; a VISA I/O library supports communication with instruments. Thus, you can still use your VXIplug&play instrument drivers and application code. The controller also supports the Agilent I/O Library suite, version 14.1.

The EX2500 lets you convert any of the eight VXI backplane trigger lines into LXI triggers through its front-panel LXI trigger-bus connectors. Therefore, you can initiate a trigger signal from a VXI instrument and have it trigger an LXI-compliant instrument. You can also use the LXI trigger as an intermediary to pass a trigger from one VXI chassis to another.

VXI Technology, www.vxitech.com.

Berkeley introduces portable power meter

Berkeley Varitronics Systems has introduced its YellowFrog power meter, which makes measurements from 800 MHz and 2.2 GHz with an accuracy of ±0.5 dB. It connects directly to the company's Gator, Dragon, Lizard, or other CW transmitters with a type N adapter for instant verification of power levels in dBm or watts.

YellowFrog can operate on two AAA Ni-MH batteries continuously for more than 8 hrs. A USB port provides both power and communication to any PC. YellowFrog includes PC controller/monitoring software for setting frequencies and recording power-out levels, but it does not require a PC to operate.

Berkeley Varitronics Systems, www.bvsystems.com.

I_{DDQ} current monitor adds on to ATE systems

Belgium's Q-Star Test has announced the transient current monitor module QT-1411 for use as an add on to any ATE to perform I_{DDQ} tests in production. The single-in-line module performs as a dynamic/transient supply current monitor and includes a digital interface and onboard memory.

The current monitor operates with any ATE in analog or digital applications. You can configure the

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monitor to measure in the ranges 5 mA to 100 A, from 2 to 50 Msamples/s, and with up to 14-bit resolution. The monitor also provides up to 3-MHz measurement repetition rate, 5-μA resolution at 5 mA, and 0.1% charge resolution on the 10-mA range. Measurement window is 20-ns minimum, 20-ms sampling at 50 MHz, or 0.5-s sampling at 2 MHz.

The monitor includes a 256-ksample internal memory, which can capture a complete current signature for off-line analysis. Driver software enables you to integrate the monitor into a test program.

Q-Star Test, www.qstar.be.

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Power analyzer figures out fluctuations and flicker

UK-based Thurlby Thandar Instruments has introduced the HA1600A power analyzer that measures line harmonics and flicker to standards EN61000-3-2 and EN61000-3-3. As an upgraded version of the earlier HA1600, the new model provides firmware to meet the latest standards, and it enables users to self-certify compliance with the standards for CE marking.

The analyzer has a 16-A current capability and uses shunt resistance of 3 mΩ. An LCD provides both graphical and numeric readout. In addition to RS-232C and USB interfaces, isolated monitor outputs provide reconstructed voltage and current signals. The analyzer provides numerical and graphical analysis of the 1st to the 40th line harmonics, which it displays as lists or histograms with compliance limits.

Thurlby Thandar Instruments, www.tti-test.com.

GPIB card transfers data at 1.5-Mbytes/s

The eAutomation Group of Advantech has introduced its PCI-1671UP, a low-cost, universal PCI/GPIB controller in MD1 low-profile form factor that allows for data transfer rates of up to 1.5 Mbytes/s. Driver and utility software allows users to control instruments from a variety of command line and programmatic interfaces.

Features include full IEEE 488.2 compatibility, a complete talker/listener controller, a 1024-word FIFO buffer, HS488 compatibility for up to 7.7-Mbytes/s data transfer to and from instruments that support the high-speed protocol, shared interrupt capability, and transparent interrupt enabling/disabling. The PCI-1671UP includes a complete NI-488.2 API and NI-VISA driver and library for support of diverse programming tools, including Visual C++, Borland C++ Builder, Visual Basic, Delphi, LabWindows/CVI, and LabView.

Base price: $470. *Advantech, www.eautomationpro.com/us.*

Analog-output devices employ USB interface

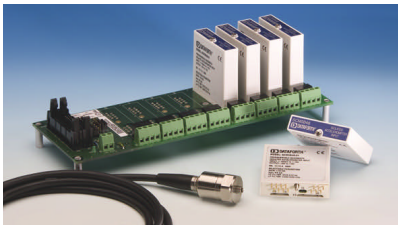
Measurement Computing's OLE_LINK1USB-3110, USB-3112, and USB-3114 16-bit analog-output devices have integrated high-drive voltage outputs, eliminating the need for external high-drive amplifiers. They are fully compatible with both USB 1.1 and USB 2.2 standards and run under Windows 2000 and XP.

The USB-3110 provides four channels of analog voltage output, eight digital I/O connections, and one 32-bit event counter. The USB-3112 has eight analog voltage outputs, while the USB-3114 furnishes 16 analog voltage outputs. Each voltage output is capable of sinking or sourcing up to 40 mA (maximum) of load current. Modules ship with a USB cable, a 5-V, 2-A AC power adapter, and InstaCal installation, calibration, and test software.

Prices: 3110—$399; 3112—$449; 3114—$599. *Measurement Computing, www.mccdaq.com.*

Signal conditioner interfaces with accelerometers

The latest member of Dataforth's SCM5B family of isolated analog signal-conditioning devices is a



field-configurable accelerometer input module. Designated the SCM5B48, the module provides excitation to piezoelectric sensors with built-in microelectronic amplifiers, commonly known as ICP or IEPE sensors.

The SCM5B48 delivers constant current excitation to the sensor, then isolates, filters, and amplifies the sensor output to yield a high-level analog voltage output. The excita-

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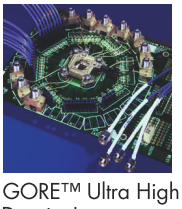

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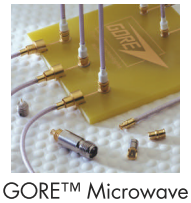

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tion current, signal gain, and filter high-pass and low-pass cutoff frequencies are field-configurable through a set of slide switches.

Six poles of signal filtering result in greater than 100 dB of normal-mode rejection for signal frequencies above the cutoff frequency. To ensure protection of data-acquisition equipment, the SCM5B48's signal inputs and sensor excitation outputs are protected against accidental connection of voltages of up to 240 V rms.

Dataforth, www.dataforth.com.

PC/104 digital I/O module is field programmable

A flexible and reconfigurable PC/104 digital I/O module, the GPIO-MM from Diamond Systems, employs a Xilinx Spartan II FPGA that allows the hardware to be reprogrammed in the field to serve multiple applications with different digital I/O requirements. Onboard flash memory stores the FPGA code and can be reprogrammed through a JTAG interface.

The GPIO-MM offers 48 programmable-direction digital I/O lines, eight fixed-input lines, eight fixed-output lines, and 10 16-bit counter/timers supported by a 40-MHz clock. Three pin headers provide a total of 100 I/O pins.

Price: $180. *Diamond Systems, www.diamondsystems.com.*

LXI video switch matrix is software-configurable

Housed in a 1U rack-mount enclosure, the Model 60-710 dual 24x8 matrix module from Pickering Interfaces switches video signals in 75-Ω transmission lines. You can also configure the 60-710 through software to operate as a single 48x8 switching matrix.

The unit's LXI Class C-compliant interface allows it to be remotely controlled through its built-in Ethernet port using a Web browser. The LXI interface serves up a soft front-panel application that lets you control the switch matrix without installing and configuring drivers. All video connections are easily accessible from the front panel.

Pickering Interfaces, www.pickeringtest.com.

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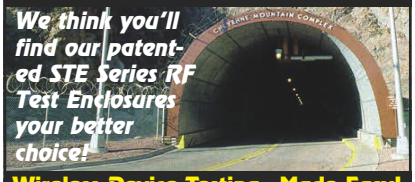

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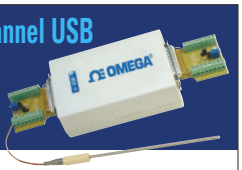

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[An exclusive interview with a technical leader]

STEVE BALDO
Global Business Unit Leader
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Steve Baldo serves as the global business unit leader for test and measurement in the Electronic Products Division of W.L. Gore & Associates. He joined Gore in 1998 as a product manager for high-speed digital interconnects and later held a number of positions, including product manager for the flagship microwave/RF test cable assemblies product line and marketing leader for test and measurement. He earned a BSEE from the University of Notre Dame and an MBA from the University of Delaware. He is also a Professional Engineer registered in the state of Delaware.

Contributing editor Larry Maloney spoke with Baldo about Gore and its products in a recent telephone interview.

A relentless drive for greater testing accuracy

Q: In 2005, *Fast Company* magazine called Gore the nation's most innovative company. What are the roots of this innovation?
A: Gore's corporate culture encourages problem solving and inventiveness, relying on teamwork and direct communication rather than cumbersome chains of command. We operate in small teams that can move with greater agility, which has served us well for nearly 50 years in obtaining hundreds of patents and reducing time to market for innovative products in diverse consumer, industrial, electronic, and medical markets.

Q: How does this approach influence the development of test products?
A: It has helped us stake out a leadership position in our microwave/RF cable test assemblies. These products deliver guaranteed phase and amplitude stability with flexure, ensuring signal integrity from the measurement instrument to the device under test. Holding calibrations for accurate and repeatable measurements allows engineers to make better decisions and assessments during product design, while minimizing downtime. We're proud that our 110-GHz test cable options won a 2005 Best in Test award in the accessory category from the editors of *Test & Measurement World*.

Q: What are some of the most common applications for these assemblies?
A: Both in metrology labs and in cutting-edge R&D settings, our VNA assemblies are used with vector network analyzers for critical measurements and device characterization. We also have a line of lightweight Gore Phaseflex cables that feature internal ruggedization. This product serves vector network uses outside the lab, such as on the production floor or on flight-line or field-test applications. The assemblies are also used in scalar analyzers, scopes, and probes. In terms of extreme demands on these assemblies, probably the most challenging area is in thermal vacuum chambers for applications in space.

Q: What is driving the growth of these products?
A: The entire market is demanding test products that will operate reliably at higher and higher frequencies, as devices get more sophisticated. Design requirements are getting more complex, which means that R&D labs are pushing the envelope in their testing. For example, we see more demanding requirements for test cable performance over temperature at higher frequencies.

Q: How do you harness the Web for customer service?
A: Engineers go to Gore's Online Store to order our most popular connector and length configurations for our test cable assemblies. There's also an online cable builder, which helps engineers identify the right cable/connector combinations for the job. Using this tool, along with our online microwave loss calculator, engineers do not have to guess when making design decisions or determining design margins. Gore provides the guaranteed and typical loss values for their specific configuration.

Q: In January, *Fortune* named Gore one of the best companies to work for—for the ninth consecutive year. From an engineer's standpoint, what makes the company so special?
A: Engineers at Gore are not entangled in cumbersome reporting systems, but rather are organized around specific projects. They are also motivated by the freedom to set their own goals, with guidance from sponsors and mentors, not bosses, to ensure alignment with company and product line objectives. This type of environment builds satisfaction and commitment, which directly relates to the cutting-edge performance and success of our products. T&MW

Steve Baldo comments on test products, customer needs, and new business ventures for product development in the online version of this interview: www.tmworld.com/2006_06.

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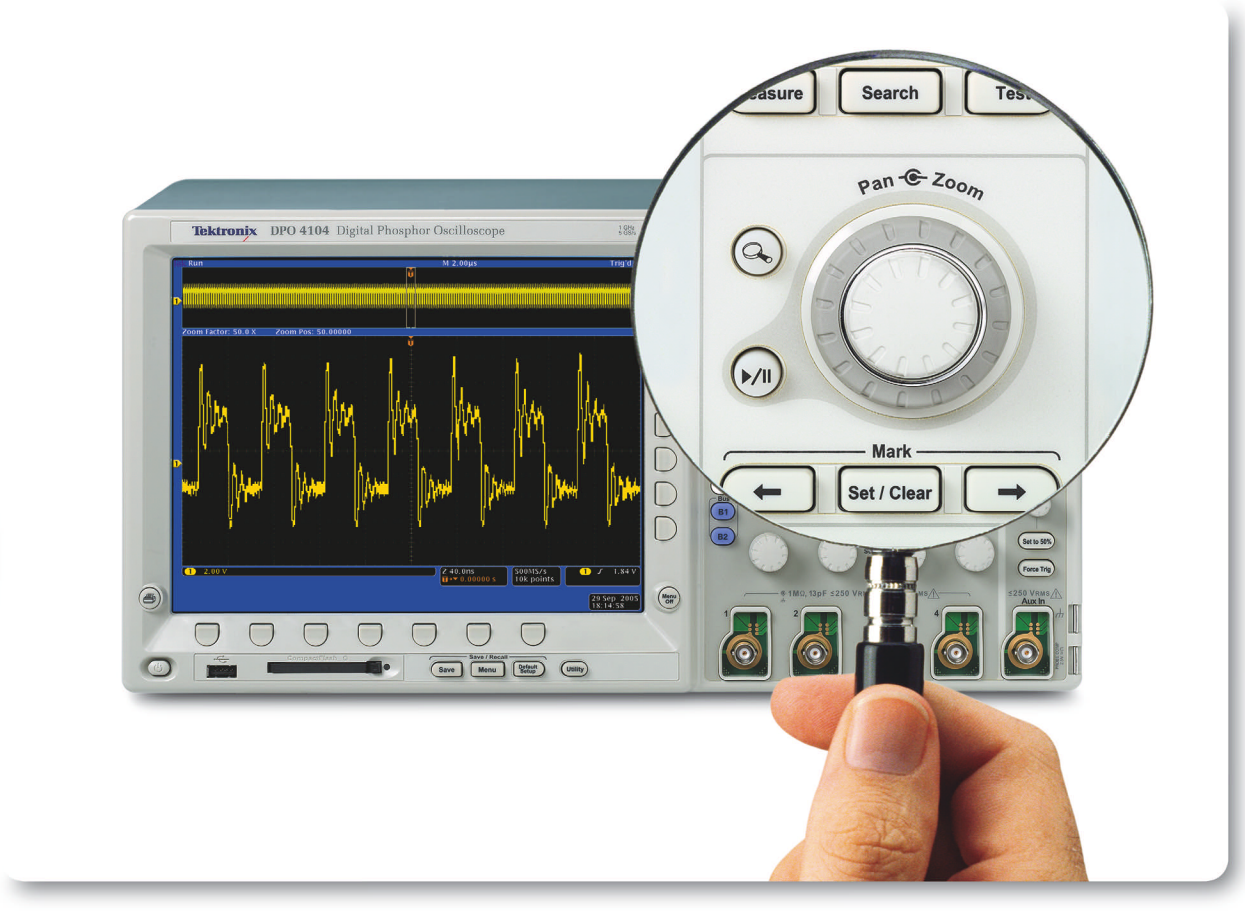

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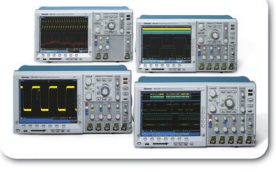

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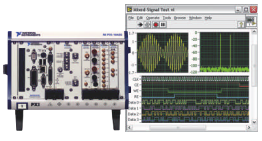

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